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Analog Adaptive Calibration for Arbitrary Phased Array Configuration

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Applying Analog Adaptive Calibration for Arbitrary Phased Array Configuration

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A thesis submitted to the faculty of
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Master of Science

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ABSTRACT

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The development of phased array antenna systems requires considerable resources and time. Due to this constraint, the Naval Air Command (NAVAIR) needs a phased array that can be physically reconfigured to meet the demands of multiple missions without added development time or cost. This work develops and demonstrates a solution to this problem by implementing an adaptive calibration approach to the development of electronically steerable antennas (ESAs). In contrast to previous analog adaptive beamformer systems, this system allows for an arbitrary antenna configuration with a variable number of antenna elements and locations. A simulation model of arbitrary phased array configurations was developed to test the beamformer calibration algorithm and was used to show practical tile locations. To demonstrate this approach, four 4x4 ULA phased array antenna tiles were built and tested together in various configurations to show the viability of developing a physically reconfigurable phased array system.

Keywords: arbitrary phased array, beam steering, beamformer calibration, electronically steerable antenna (ESA), analog beamforming, adaptive beamforming

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I am very grateful for all the help I have received from fellow students who have helped on this project, namely Trevor Schwantes, Justen Gardner, David Buck, Jason Burrows, Travis Bonner, and especially Jakob Kunzler. Jake's work in keeping the project moving during my absence was a lifesaver for us in getting ready for our demonstration. I have learned a lot from my work with each of these students.

I would like to thank each of my committee members: Dr. David Long and Dr. Brian Jeffs for their help and advice. I also want to thank my advisor Dr. Karl Warnick for all of his guidance and assistance over the last three years of being a member of his research group.

I am grateful to my parents and family for all their support over the six years of my college experience.

This work was supported and coordinated by Navair and I have had the privilege of working with Brent Hedman as the project sponsor. I have learned a lot from our interactions, and I am very grateful for the financial support.

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CHAPTER 1. INTRODUCTION

Phased array antenna transmitters contain multiple radiating elements that are combined to create a more directive antenna that is an electronically steerable antenna (ESA). ESA systems have existed for many years but are limited in their applications because of the large development cost. This work explores a new way of building a phased array transmitter that has the potential to greatly reduce the cost and development time by building smaller modular antenna tiles that can be added together to increase the equivalent isotropically radiated power (EIRP). This reduces development cost by allowing for system reuse and reconfiguration with design flexibility. Using a simple antenna building block, this system has the potential to create ESAs with up to 1728 antenna elements in different configurations. This work has been sponsored by the Navair Air Systems Command (Navair).

1.1 Project

1.1.1 Design Goal and System Requirements

The Naval Air Systems Command (Navair) is formally a branch of the Navy. In support of their mission [3], their research labs in China Lake, CA have identified a need for a low-cost, mobile, quick-to-deploy, and somewhat disposable phased array system to simulate ground radar systems in their fighter-jet test range.

The sponsor-given system requirements are listed as the following:

- be low-cost (disposable)
- be mobile
- use only commercially available parts
- be reconfigurable for use in multiple missions

- radiate as much power as legally possible (maximize EIRP)
- demonstrate phased array beamsteering

This work fulfills of all these requirements. With the helpful guidance of my advisor, Dr. Warnick, I chose other important system parameters. In this project, I worked with other research students to meet these requirements by investigating the possibility of building a modular phased array transmitter constructed from aggregate antenna tiles acting under central control. The results from the initial contract or phase 1 have demonstrated the feasibility of four antenna tiles working together. The successful demonstration of four tiles has already led to another year of funding for phase 2 which will scale the hardware to eight or more tiles.

1.2 Motivation

The first published phased array antenna design was demonstrated by engineers working for Hughes Aircraft Company in 1958 with the first electronically steerable antenna. In several ways, the phased array antenna pre-dates the satellite dish [4] but difficult challenges have kept it from being widely used in antenna systems. Phased array antenna systems have existed for decades as expensive antenna systems that take years to develop. For these reasons, they have largely stayed out of the hands of consumers, and most applications for phased array technology have been associated with the military. The focus of this work is to develop an antenna system for the military that demonstrates the required functionality and does not cost millions of dollars.

Antenna technology has changed dramatically since Hertz's first successful radio transmission in the 1880's. The world has evolved around the need for dynamic technology that responds to our every command. Users of today have become accustomed to cell phone and computer technology that responds quickly with minimal user interaction. Satellite communication technology has fallen behind other areas of technology in innovation simply because of the high cost of development. Early development of satellite technology cost companies hundreds of thousands of dollars or more. This high cost to market limited early innovation to large companies and governments that could afford the price.

Parabolic reflector antennas are still commonly used for satellite telecommunications today. These satellite dishes started out at about 6 meters across (20 feet) in about 1978, but slowly over

the last three decades, the needed size dropped to the well-known dish size, 20 cm (about 8 in) across. While many improvements have been made with different parts of satellite communication over the years, steerability is one thing that has mostly stayed mechanical in nature.

The steerability of an antenna refers to how easy it is to redirect the main lobe of antenna radiation. The problem with the typical satellite dish is that it needs to be physically pointed at the right point in the sky for it to work. For decades, different solutions have been created to steer a satellite dish. Often the steering is not automated at all and thus steered by a human, or if it is automated, it uses motors that can take up to fifteen minutes to search the sky for the satellite. While working as an intern for the Raytheon^{TM}Company in Largo Florida, I personally experienced this type of automated solution to satellite telecommunication antenna technology. This slow satellite acquisition time shocked me! As I reflect on that experience, I see this latency of satellite acquisition as a serious vulnerability to the soldiers effected by that satellite dish. Imagine if that dish needed to send a life-saving message. Waiting fifteen minutes could be too late. Mechanically steered satellite dishes will always be limited in how fast they can search the sky. We need to throw out the dish and develop a new standard of satellite telecommunication.

The literature review in Section 1.3 considers how phased array antennas can be a solution to this problem. Navair needs a cost-effective high gain antenna that can be steered with a computer and can be dynamically configured. As part of the military, Navair is already accustomed to building expensive antenna systems. This work introduces a modular approach to lowering the cost of a phased array transmitter. The modular approach allows the user, Navair in this case, to link multiple antenna tiles to achieve the required EIRP for the given mission.

1.3 Previous Work

Since Spradley's first demonstration in 1958 [4], the concept of phased array antennas has grown to become a vast research area respected across the globe. Many different architectures exist for phased array antennas, but broadly considered they are either analog beamforming, digital beamforming or some hybrid of the two. There are advantages and disadvantages to both types of phased array antenna systems.

1.3.1 Analog Phased Array Antennas

As the history of Electrical Engineering has evolved, analog systems have always predated their digital counterparts. The reasoning for digital systems coming later may seem obvious; early computing systems were not powerful enough to even consider the option. For this reason, the earliest phased array systems were analog-controlled. The simplicity of these systems has led to their continued development for decades. For example, Ohira reviews multiple architectures for analog-controlled ESAs in [2].

Figure 1.1 shows one of the simplest topologies for analog-controlled ESA design discussed by Ohira. Here microwave phase shifters are used to steer the antenna. This is considered analog because the phase shifting is controlled in the circuitry. The hardware built in this project reflects a similar architecture and uses discrete phase shifters to accomplish the phase shifting showing Figure 1.1.

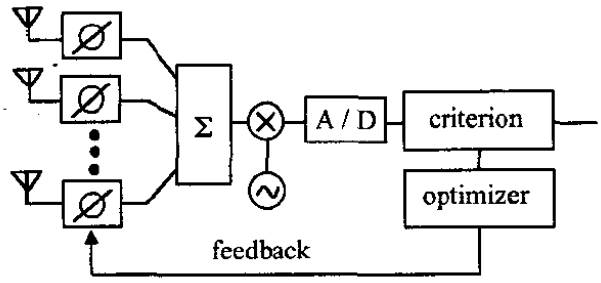

Figure 1.1: Analog Phased Array Antenna Topology using variable phase shifters [2].

1.3.2 Digital Beamforming

The digital form of phased array antenna systems has an even simpler architecture than shown in Figure 1.1 because the phase shifting, summing and signal processing all happens inside the computing system. This is called digital beamforming and in many ways is more capable than its analog counterpart. Authors Van Veen and Buckley review multiple digital beamformers in [5], namely the Max-SNR and other statistically optimal beamformers.

1.3.3 Analog Adaptive Beamforming

Many papers have studied adaptive beamforming as a fully digital beamformer solution. This project has demonstrated an adaptive beamformer that implements the phaseshifting in RF hardware. This so called analog adaptive beamformer is similar to the approach presented by Ohira [6] [7]. Ohira shows the difference between digital beamforming and analog beamforming and presents a similar topology to Figure 1.1.

In contrast to Ohira's work in Japan, Dugger et al. [8] have demonstrated analog adaptive beamforming with audio using two microphones. The filter block discussed in their work is directly analogous to the analog phase shifters used in this project. Our transmit-only system was not required to measure the noise environment, therefore our system cannot place nulls like Dugger et al. did in the traditional form of adaptive beamforming as discussed by Buckley and Van Veen in their review paper [5].

Finally, Hossu et al. [9] [10] implemented an analog adaptive beamforming system for satellite tracking and experimentally compared it to a fully digital system. Their satellite tracking application is more advanced than this project, but their zero-knowledge approach is similar ours. This project has "zero-knowledge" about the antenna array geometry and the phase length of each path.

1.4 Contribution

The contribution of this thesis is summarized in the following list:

- Presented a modular approach to analog adaptive beamforming calibration that allows for system reconfiguration and reuse using a "Zero Knowledge Approach" for the array geometry.
- Implemented and demonstrated the necessary hardware and digital platform of an analog adaptive beamformer.
- Vetted the low-cost homemade antenna chamber that is in use by our research group.

These efforts include the development of eight custom designed PCBs, five of which worked at X-Band frequencies. These boards will be discussed in detail in Chapter 3.

This work was completed as part of a group effort with as many as five undergraduates (for a short time) working with me as their project leader. I taught and mentored four of these students in the development of different aspects of the design. My personal contributions to this project as a whole are summarized in the following list:

- Designed and laid out 40 iterations of the PCBs used in this project.
- Developed the full firmware platform in Vivado 2016.2.
- Developed the low-level software drivers (including the phase shifter control) and the UI class.
- Performed hardware system integration and all hardware debugging of each of the antenna tiles.
- Conducted experimental measurements and the analysis of the results.

1.5 Thesis Outline

This thesis is organized as follows:

Chapter 2: Background, discusses the basics of phased array antennas and formally presents the overlap integral formulation used in the simulation of the Navair system.

Chapter 3: Hardware Development, gives an overview of the hardware developed over the course of the project

Chapter 4: Software Development, gives an overview of the software developed over the course of the project. It includes a discussion about both the firmware and the bare-metal software.

Chapter 5: Experimental Results, examines experimental results from the system with a discussion of the experimental setup.

Chapter 6: Conclusion, discusses the lessons learned from this project and future work that can be done.

CHAPTER 2. BACKGROUND

2.1 Phased Array Antenna Basics

Phased array antenna systems contain multiple radiating elements that are used together to create a more directive antenna that is steerable. The simplest case of a phased array is the uniform line array (ULA) or simply a line of antenna elements a fixed distance apart. Figure 2.1 shows a uniform line array with four antenna elements on the z-axis all simultaneously receiving RF radiation from the far field. The far field is an approximation that says when RF radiation is many wavelengths away from the antenna (ten or more wavelengths), then we can approximate that the angle is the same for each antenna element. The radius, R, between each element and the source of radiation is shown and the triangle formed has an angle θ, with the z-axis. The right triangle formed between Z_1 and Z_0 in Figure 2.1 shows that the signal traveling to Z_0 must travel an extra distance of $d\cos\theta$ in comparison to Z_1. The extra distance traveled constitutes a different electrical length, and thus the signal that arrives at Z_0 has a different phase.

Phased array systems exploit this phase difference by manipulating the phase of signals either digitally or in analog using circuitry to add different phase lengths. In the hardware built for this project, we used a phase shifter which adds variable amounts of electrical length to achieve analog phase shifting. This allows us to build an electronically steerable antenna as shown in Figure 4.1.

2.2 Classical Analysis: The Array Factor Approximation

The classical way to approach the analysis of a phased array system is to "represent the field radiated by the array as a product of the radiation pattern of one element and an array factor that includes the locations and excitations of each element in the array" [11, p.123]. The method has been used for decades and allows for pencil and paper calculations about phased array, but

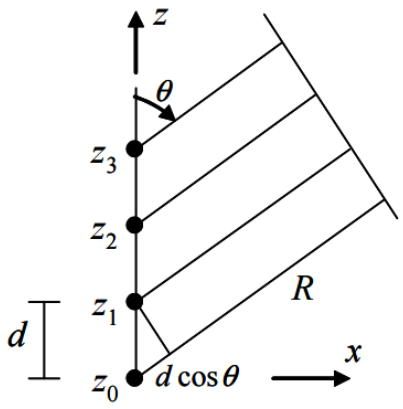

Figure 2.1: Far field phase uniform line array (ULA) diagram showing four antenna elements along the z-axis with a wave coming in at an angle of θ.

this method neglects the effects of mutual coupling within the array which causes the radiation pattern to differ across the array. In Section 2.3 we discuss a more sophisticated method that includes mutual coupling but at the price of requiring numerical approximations and thus cannot reasonably be calculated on paper. The following is a mathematical treatment of the array factor adapted from [11].

First, we must consider the element pattern of a single antenna placed at the origin of the coordinate system and excited with a driving input current I_o such that the antenna equivalent current source is $\overline{J}$. Using the far-field radiation integral, the radiated far field is

$$\overline{E}_{\text{el}}(\overline{r}) = -j\omega\mu(1-\hat{r}\hat{r})\frac{e^{-jkr}}{4\pi r}\int d\overline{r}' e^{i\vec{k}\cdot\vec{r}'}\overline{J}\left(\overline{r}'\right), \tag{2.1}$$

where $\overline{k} = k\hat{r}$. If the antenna is shifted to the point $\overline{r}_1$, the field becomes

$$\overline{E}(\overline{r}) = -j\omega\mu(1-\hat{r}\hat{r})\frac{e^{-jkr}}{4\pi r}\int d\overline{r}' e^{j\overline{k}\cdot\overline{r}'}\overline{J}\left(\overline{r}'-\overline{r}_1\right) \tag{2.2}$$

$$= -j\omega\mu(1-\hat{r}\hat{r})\frac{e^{-jkr}}{4\pi r}e^{j\overline{k}\cdot\overline{r}_1}\int d\overline{r}'' e^{j\overline{k}\cdot\overline{r}''}\overline{J}\left(\overline{r}''\right) \tag{2.3}$$

$$= e^{j\overline{k}\cdot\overline{r}_1}\overline{E}_{\text{el}}(\overline{r}). \tag{2.4}$$

This demonstrates the Fourier shift theorem, since a shift in the near field location of the antenna becomes a phase shift in the far field.

If we have an array of N identical elements driven with phasor excitation currents $i_1, i_2, \ldots, i_N$ and located at the points $\bar{r}_1, \bar{r}_2, \ldots, \bar{r}_N$, the total field can be found by summing the field from each element, with scaled input currents on each element (i.e. $i_{\text{in}} = i_n$ rather than $i_{\text{in}} = I_{\text{o}}$). The combined far-field is

$$\overline{E}(\bar{r}) = \sum_{n=1}^{N} \frac{i_n}{I_0} e^{j\bar{k}\cdot\bar{r}_n} \overline{E}_{\text{el}}(\bar{r}) \tag{2.5}$$

$$= \overline{E}_{\text{el}}(\bar{r}) \underbrace{\sum_{n=1}^{N} \frac{i_n}{I_0} e^{j\bar{k}\cdot\bar{r}_n}}_{\text{Array factor } A(\theta,\phi)} . \tag{2.6}$$

This result is powerful because the radiation pattern of the array is factored into a product of a single reference antenna and an array factor that packs array information together - the antenna locations, and the phases and amplitudes of the current at each element.

2.3 Overlap Integral Formulation

The overlap matrix is a mathematical formulation for phased array antenna patterns that avoids the need to calculate full wave solutions for multiple elements. The overlap matrix is better than the classical array factor approach because it accounts for mutual coupling between antenna elements. This material is adapted from [11].

First, we need to define the array beamformer weights for a transmitting array as a column vector

$$\mathbf{w} = \begin{bmatrix} I_1^* \\ I_2^* \\ \vdots \\ I_N^* \end{bmatrix}, \tag{2.7}$$

where I_n is the phasor input current into the nth array element. The beamforming software manages this vector and the variable phase shifter settings after the beam has been calibrated.

In terms of embedded element patterns $\overline{E}_n$ and the beamformer weight vector W, the total radiated electric field for a transmitting array is

$$\overline{E}(\bar{r}) = \frac{1}{I_0}\sum_{n=1}^{N} w_n^* \overline{E}_n(\bar{r}). \tag{2.8}$$

Using this result we can evaluate the total radiated power of the phased array system:

$$P_{\text{rad}} = \frac{1}{2\eta}\int |\overline{E}(\bar{r})|^2 r^2 d\Omega \tag{2.9}$$

$$= \frac{1}{|I_0|^2}\frac{1}{2\eta}\int \sum_{m=1}^{N} w_m^* \overline{E}_m(\bar{r}) \cdot \sum_{n=1}^{N} w_n \overline{E}_n^*(\bar{r}) r^2 d\Omega \tag{2.10}$$

$$= \frac{1}{|I_0|^2}\sum_{m=1}^{N}\sum_{n=1}^{N} w_m^* \underbrace{\frac{1}{2\eta}\int \overline{E}_m(\bar{r}) \cdot \overline{E}_n^*(\bar{r}) r^2 d\Omega}_{\text{Overlap integral}}. \tag{2.11}$$

From the previous derivation we can now formulate the element pattern overlap matrix $\mathbf{A}$ with elements given by:

$$A_{mn} = \frac{1}{2\eta}\int \overline{E}_m(\bar{r}) \cdot \overline{E}_n^*(\bar{r}) r^2 d\Omega. \tag{2.12}$$

If all the elements are identical and we neglect array edge effects, then the diagonal elements A_{mn} are equal and represent the power radiated by the array with input current I_0 into the nth element port and the other ports open circuited. In matrix notation, the total radiated power becomes

$$P_{\text{rad}} = \frac{1}{|I_0|^2}\mathbf{w}^H \mathbf{A}\mathbf{w}. \tag{2.13}$$

To compute the directivity of an array, we also need the radiated power density in a given direction. The radiated power density can be placed into matrix form using

$$S_r(\bar{r}) = \frac{1}{2\eta}|\overline{E}(\bar{r})|^2 \tag{2.14}$$

$$= \frac{1}{2\eta\,|I_0|^2}\left|w_1^*\overline{E}_1 + w_2^*\overline{E}_2 + \cdots + w_N^*\overline{E}_N\right|^2 \tag{2.15}$$

$$= \frac{1}{2\eta\,|I_0|^2}\sum_m w_m^*\overline{E}_m \cdot \sum_n w_n\overline{E}_n^* \tag{2.16}$$

$$= \frac{1}{|I_0|^2}\sum_{m,n} w_m^* \underbrace{\frac{1}{2\eta}\overline{E}_m \cdot \overline{E}_n^*}_{B_{mn}(\bar{r})} \tag{2.17}$$

$$= \frac{1}{|I_0|^2}\mathbf{w}^H\mathbf{B}(\bar{r})\mathbf{w}, \tag{2.18}$$

$$\tag{2.19}$$

where the directivity is the direction of the far-field point $\bar{r}$.

By combining the total radiated power and the power density, we can express the directivity as

$$D(\Omega) = \frac{4\pi r^2\mathbf{w}^H\mathbf{B}(\bar{r})\mathbf{w}}{\mathbf{w}^H\mathbf{A}\mathbf{w}}. \tag{2.20}$$

The above formula was used in our simulated model with various beamformer weights to approximate the antenna element pattern with various numbers of elements and with arbitrary element locations.

2.4 Summary

Understanding the basics of phased array signal processing is important for the considerations made in this thesis. The basics presented in this chapter require previous knowledge about the phased array geometry (the "d" vector in Figure 2.1) and thus can be considered an a priori calibration. The simulation model used in this thesis uses the a priori phased array signal processing techniques from this chapter and was developed using the array factor approximation and expanded using the overlap integral formulation. As discussed later in Chapter 4, our system differs from the a priori calibration presented in this chapter by using an a posteriori calibration method

that requires “Zero-Knowledge” about the array geometry. A posteriori array calibration methods have been presented in past [12], but this work allows the array to be reconfigured and calibrated quickly.

CHAPTER 3. HARDWARE DEVELOPMENT

3.1 Introduction

The goal of the hardware developed in this project was to demonstrate analog adaptive beamforming with multiple phased array antenna systems using a "zero-knowledge" approach that was previously discussed. The limited requirements we received from the project sponsor were to build an ESA transmitter that was "low-cost, mobile, quick-to-deploy, and somewhat disposable" (see Section 1.1.1). To achieve this goal we needed to prototype a phased array antenna system that could be duplicated several times with repeatable results.

The antenna tile hardware design was driven by our limited requirements within the scope of our research goal to quickly calibrate multiple phased array antennas simultaneously. We built off lessons learned in a previous BYU research project. The "OverHorizon" project was proprietary research project to develop a Ku-band dual-polarized Transmit/Received (T/R) satellite communication system. Both the OverHorizon project and the system discussed in this work used analog phase shifters to accomplish phase shifting. Our system was designed as an X-band radar at 10.25 GHz instead of Ku-band. Starting Fall 2017, we prototyped new hardware that was pieced together into what we called an antenna tile, which consisted of a 4x4 patch antenna, a blade for each element (see Section 3.3) and a 1 to 16 power divider.

3.2 Power Divider

The hardware design required the development of a 1 to 16 power dividing network that was space efficient. Initial efforts for this part of the project used a cascading network of 1 to 2 Wilkinson power dividers [13, pp. 328-332]. This approach produced successful experimental results but was later rejected due to lack of space efficiency on the printed circuit board (PCB). We decided to experimentally design a 1 to 16 T-Junction power dividing network [13, pp. 324-

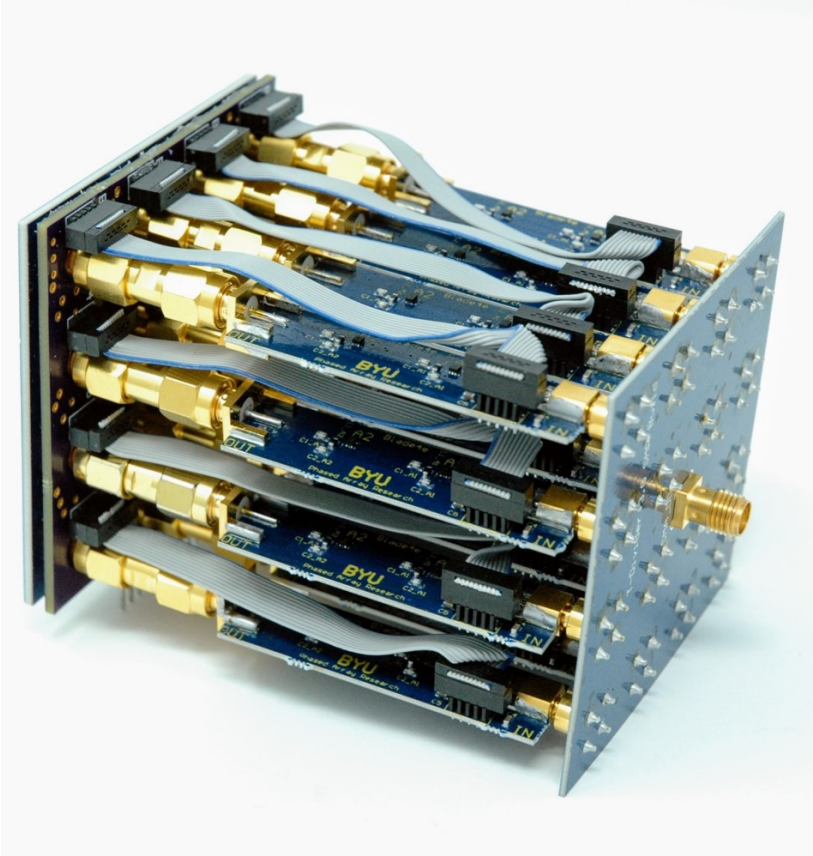

Figure 3.1: A photograph of a finished antenna tile. Many tiles can be used together to form an aggregate array.

328] using the HFSS modeling software. This decision was chosen because of the efficient PCB layout associated with T-Junction. Despite the advantages of using the T-Junction, our engineering decision came with a couple of drawbacks. In contrast to the Wilkinson power divider, the T-Junction power divider is not matched at every port, as discussed in greater detail by Pozar [13]. For this reason, we used a microstrip Quarter-Wave transformer [13, pp. 72-75] to match the forward looking input impedance port to a characteristic impedance of 50 Ω.

Our design decision to use a T-Junction power divider was only possible because we were asked to build a transmit-only system. The T-Junction power divider is reciprocal but in general is not matched on the output ports. In designing for a transmit-only system we were able to mitigate the problem of using the T-Junction power divider by using an amplifier chain that approached the unilateral approximation for amplifier design [13, pp. 541]. The unilateral approximation for amplifiers assumes that the wave is one directional through the amplifier and that the reverse wave

is negligible. In this case the s-parameters for a unilateral amplifier with input port 1 and output port 2 are the following:

$$\begin{bmatrix} S_{11} & \approx 0 \\ S_{21} & S_{22} \end{bmatrix},$$

where S_{12} is negligibly small and S_{21} is the gain parameter of the amplifier. This approximation is important because of the lack of input matching at each of the 16 ports at the output of the power dividing network.

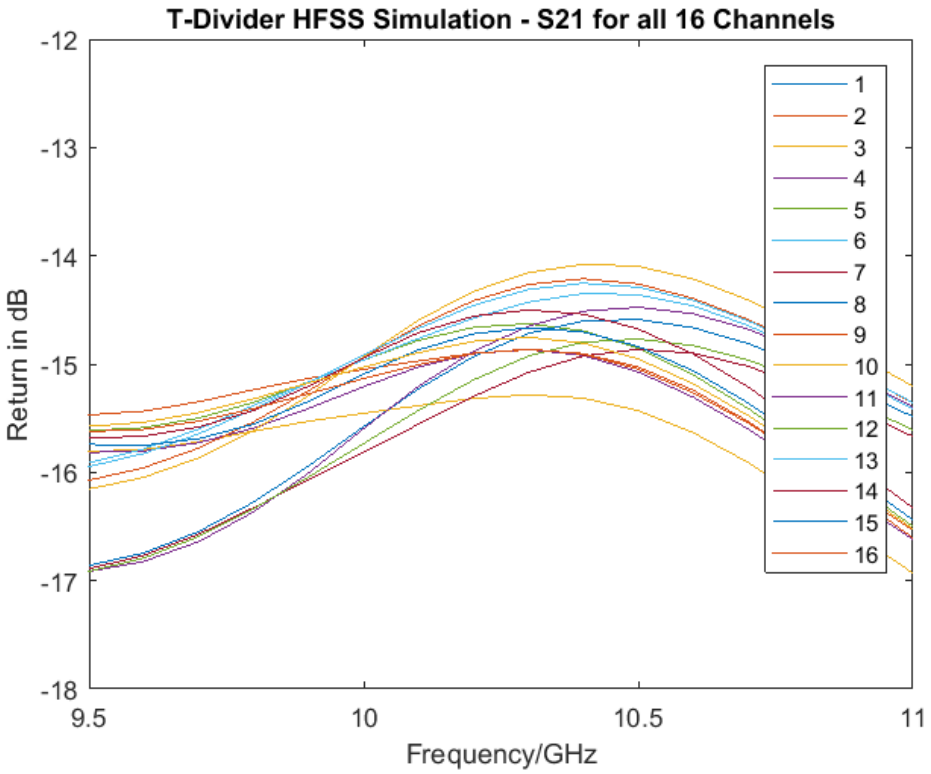

Figure 3.2: HFSS Simulation of S21 through the T-Junction Power Divider showing that the loss in each of the 16 channels is between 14dB and 16dB in our desired band.

Our simulation in the commercial modeling software HFSS from Ansys showed promising results. We optimized the microstrip geometry to minimize the excess loss through the power divider. A lossless power divider would split the signal perfectly in half (-3dB). In a 1 to 16 power divider there are effectively four divisions, meaning 12 dB of loss is expected. Figure 3.2 shows a simulation that anticipated between 14dB and 16dB of loss through the splitter. Figure 3.3 shows

the fabricated board from Quickturn Circuits. Figure 3.4 shows that we were able to beat the simulated loss by about one dB because of unmodeled coupling in the simulation. The results in Figure 3.4 show that there is only about one to three dB of excess loss through the splitter, which is much better performance than any reasonably-priced commercially available option.

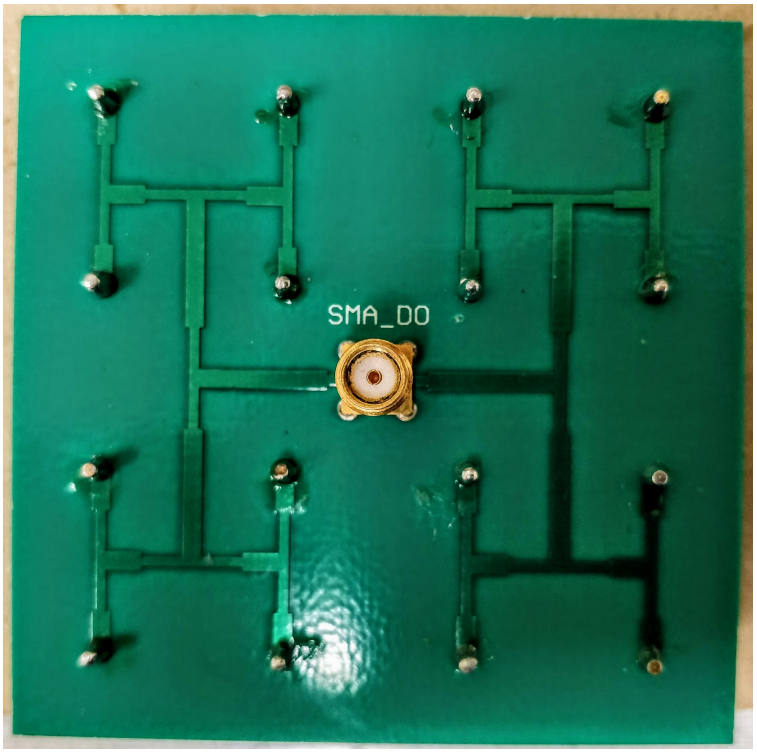

Figure 3.3: A working prototype board of our T-Junction power divider.

3.3 Blade

The hardware developed for this project was influenced by a previous satellite communications project funded by OverHorizon (currently branded as Ovzon). During the OverHorizon research project, we developed an eight-element dual polarization transmit array antenna system that met similar requirements to the Navair project. Thus, the Overhorizon transmit array was used as the basis for the Navair project but only in a single polarization. The Overhorizon hardware architecture had a distributed architecture where each board contained one step of the signal chain for each channel. For example, there was one board for all of the phase shifters which connected

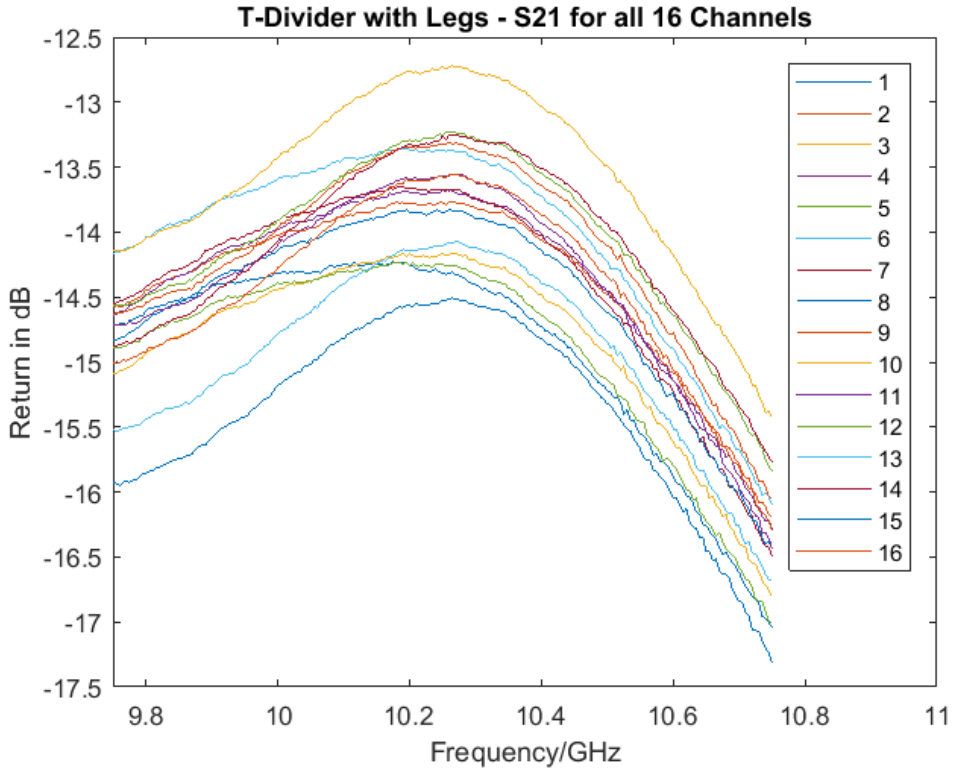

Figure 3.4: The measured S21 through the T-Junction Power Divider showing that the measured loss in each of the 16 channels is between 13dB and 15dB. This measurement shows less loss than the simulation because of unmodeled coupling which in this board is desirable.

to another board that contained all of the power amplifiers and so on. While this architecture is useful in many ways, it proved to be major problem during the hand manufacturing process. While building these boards with chips that were quite expensive, the hand soldering process led to weeks of continual rework to get all of the channels working at the same time. The electronics density was such that fixing one of the chips (e.g., a phase shifter: MAPS-010146) would cause a neighboring chip to reflow that also need to be reworked. Building off this experience, the distributed architecture was rejected during the planning stages of the Navair project.

Early in the design process, we decided to fundamentally change the signal path from our previous work in the OverHorizon project and to move to a single channel signal chain referred to as a blade architecture. The blades were designed to support all of the necessary circuitry for one of the antenna elements in the phased array. Each blade contains one digitally-controlled phase shifter (MAPS-010146), two power amplifiers (MAAM-011101) and the necessary circuit elements for

the before mentioned chips. The design went through 5 major prototype iterations and many minor iterations. Figure 3.5 shows a picture of a working blade. After months of work, the design converged on a blade design that has between 13.7 dB and 14 dB of gain and SPI-controlled phase shifting capability (for more information about the phase shifting control software please refer to Sections 4.4 and 4.5). Figure 3.6 shows the measured gain (S21) on a single working blade and is characteristic of all the blades used in the final product.

While the blade hardware design is considered mature, I would suggest some changes for future work after having made 64 working copies of the final design (also see Section 6.2). The power amplifier (MAAM-011101) was chosen primarily to save cost but the smaller TDFN package has proven to be a serious problem. In consulting with others in industry, we were encouraged not to use this amplifier in our design. When we asked a professional to solder our boards (to save time), he rejected the build because of the hours of rework needed to correctly solder this part. Future redesigns of the blade should reject this amplifier to improve solderability and design stability. The phase shifter used in this design (MAPS-010146) is still considered the best option for digitally-controlled phase shifting between 8 to 12 GHz.

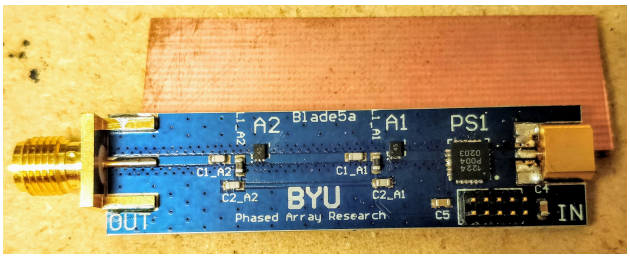

Figure 3.5: A working prototype board of the blade design.

3.4 Digital Interconnect Board

This board was simply designed to be the interface between the digital controller and each of the blades. This board is also used for power distribution for the biasing voltages on the phase shifters and the rf amplifiers. This board is shown in Figure 3.1 sandwiched between the antenna and the SMA-ports. As shown, this board has 16 ribbon cables that connect to each of the 16 blades and two ribbon cables (not shown) that bring the digital and power lines to this board from

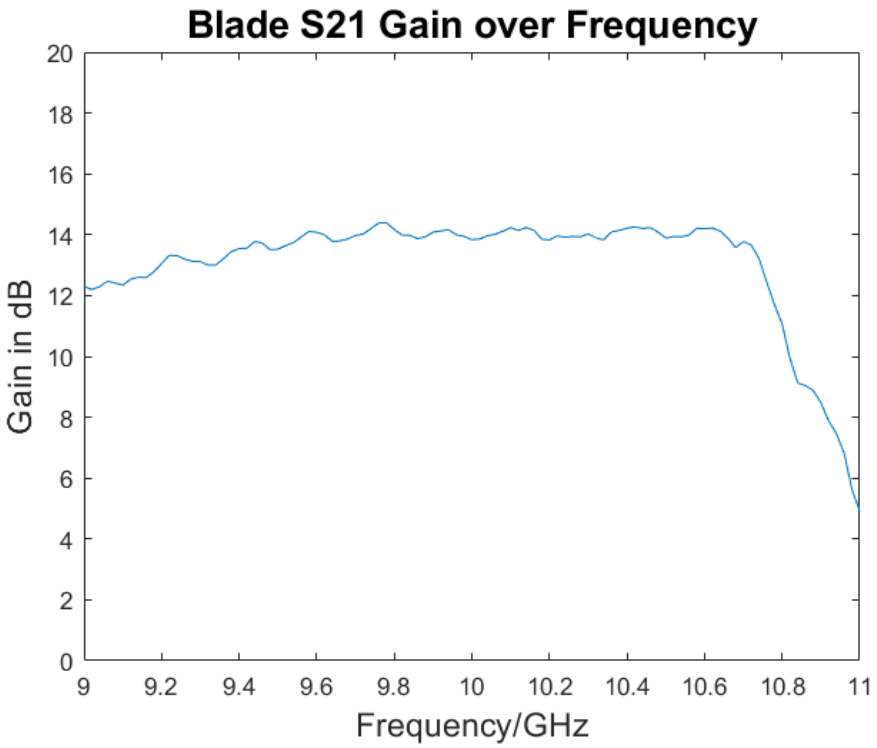

Figure 3.6: Measured S21 gain of a working blade showing a relatively flat gain response between 9.5 and 10.8 GHz of about 14dB.

the breakout board (see Figure 5.2). This board is not shown as a yellow block in Figure 5.2 but rather distributes the red and blue wires to the antenna tiles shown along the top of the figure.

3.5 Antennas

The antennas used as the driving elements in the transmit array designed for the Navair project were designed using Ansys' tool called HFSS. A uniformly spaced patch antenna was tuned to 10.25 GHz to be well centered across the FMCW band for our radar pulse (10 to 10.5 GHz). For a narrower main lobe of antenna radiation, the element spacing was chosen to be 0.55λ or about 1.61 cm. This deviation from half λ element spacing represents a fundamental trade off in this antenna design that was decided by David Buck. Using Dr Warnick's Matlab-based modeling library, David chose a narrower half power beamwidth of 2 degrees, and in so doing raised the maximum sidelobe level by .32 dB. This early design decision helped focus the antenna design on the goals of the sponsor, Navair, by focusing on the mainlobe and not worrying about sidelobes. The analysis for this decision will be documented later in David Buck's PhD dissertation.

Figure 3.7: A working prototype board of the 4x4 patch antenna design.

3.6 Circuit Board Fabrication

Each of the antenna tiles developed during the Navair project consisted of 19 custom PCBs that were designed, laid out and soldered by members of the Smart Antennas Research group. This custom hardware constituted most of the effort and included about seven months of PCB prototyping and testing. While the elements of this hardware design are generally considered routine RF engineering and not cutting-edge research, novel design techniques were used to create the final product shown in Figure 3.1.

The hardware developed during the Navair project was designed in Altium 17/18 with detailed schematic capture. The RF PCBs for this project were all fabricated by Quickturn circuits (QTC) in Salt Lake City, UT and the digital interconnect board was fabricated by OSHPark. The parts were ordered from multiple suppliers online including Digikey, Mouser, Newark and others. A professional assembler located in North Salt Lake City named Danny Blackburn helped with the soldering of 24 of the blades but the rest of the boards were soldered by research students in the Smart Antenna Systems group.

3.7 Summary

The hardware developed for this project was built to demonstrate analog adaptive beamforming with multiple phased array antenna systems using a “zero-knowledge” approach. The

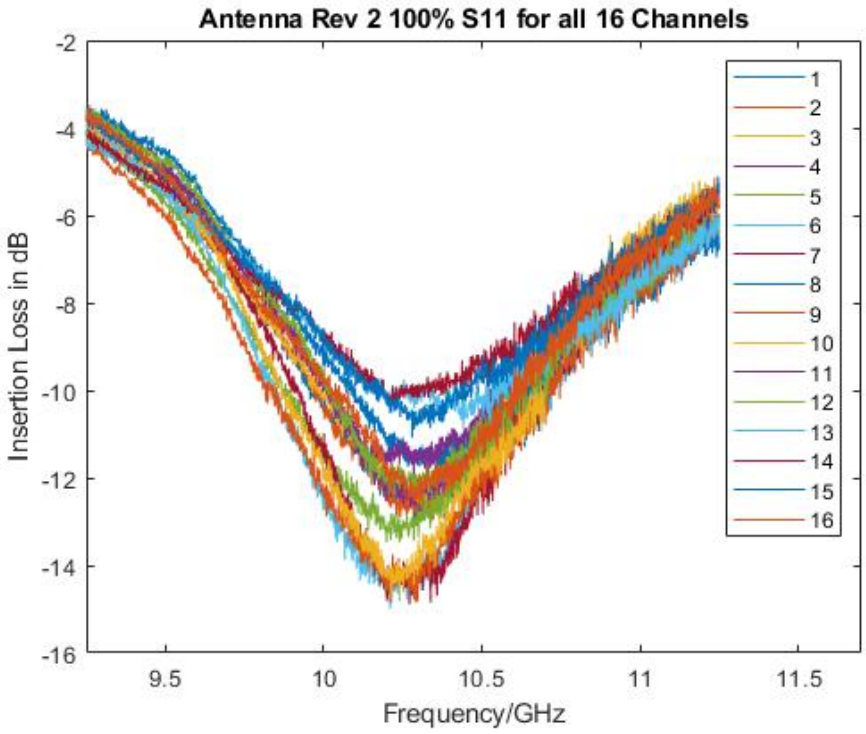

Figure 3.8: Measured insertion loss of all 16 channels of the working 4x4 patch antenna array showing an average s11 of -12.25 dB that is tuned around 10.25 GHz.

PCBs developed for this project were prototyped over a seven month period and produced four functioning antenna tiles. Our goal in building the hardware was to develop PCBs that would be easy to duplicate thus simplifying the process of building multiple antenna tiles. Using a "blade" topology simplified this process by allowing us to validate each channel individually. The next phase of this project will likely reuse most of the elements of the hardware presented in this chapter except for the blade PCB which needs a different power amplifier.

CHAPTER 4. SOFTWARE DEVELOPMENT

4.1 Introduction

The software platform developed in this project was used to drive the hardware described in the Chapter 3. The blade PCB consisted of a phase shifter for each antenna element in the array (see Section 3.3). Figure 4.1 shows our design decision to use one phase shifter per antenna element to electronically steer the beam of this fully populated antenna system. Other system designs can use fewer phase shifters but always at the cost of performance. For example, it is not necessary to populate every antenna element with the required RF hardware in a thinned array. In our case, we did populate every element and thus needed to manage the control of many discrete phase shifter chips. The goal of this software platform was to optimally drive each of the phase shifters to form the maximum directivity beamformer. This goal was accomplished by developing a single processing system with enough input/output (I/O) to drive all of the antenna tiles simultaneously.

Borrowing on experience from the Overhorizon research project (see Section 3.3), a discrete phase shifter chip was chosen to help with this I/O management problem. Most commercial phase shifters on the market have multiple bits of phase resolution (4 bits in our case), but we found it was very common for each of these bits to be individual discrete inputs. It was easy to see early on that this many I/O would quickly become unmanageable as the project progressed through its goal of testing multiple antenna tiles together. The phase shifter that we chose was made by MACOM (PN: maps-010146 [14]) and was special in that it allowed for parallel control using the Serial Peripheral Interface (SPI) protocol. Use of this SPI protocol and an FPGA allowed this research effort to dramatically decrease the I/O needs and the PCB layout constraints.

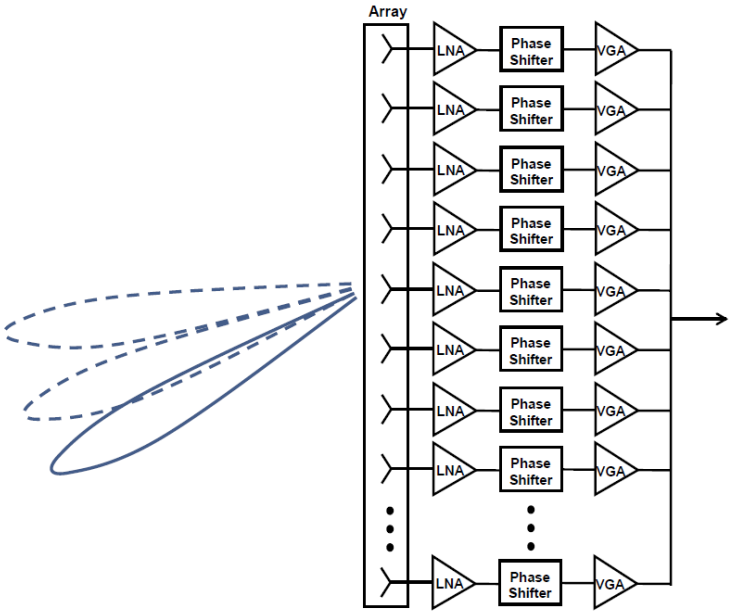

Figure 4.1: General analog beamformed ESA block diagram.

4.2 Adaptive Beamforming

The innovative effort of the Navair project was to aggregate multiple phased array antenna systems together to maximize EIRP. This aggregate system obtained met our given requirement (see Section 1.1.1) of being reconfigurable and thus will lower the potential development cost through reuse in multiple missions. The reconfigurable nature of this system was implemented by developing a digital system that optimizes the ADC input relative to the current phase shifter values. These phase shifter values are analogous to the beamformer weights discussed in Chapter 2 but this work does not attempt to show this connection mathematically. The optimization of the phase shifter values was demonstrated with the experimental test setup explained in Chapter 5 and shown in Figure 5.1.

Our efforts in this project show the ability to arbitrarily locate multiple phased array systems together and form the maximum directivity beamformer without having to precisely know the element locations. Neither the firmware nor the software discussed in this chapter have prior knowledge of the antenna element positions and thus traditional beamforming techniques, like the array factor method, cannot be used.

Instead of using an array factor, the bare-metal software runs an optimization algorithm looking for the global maximum input ADC reading from the power detector. As discussed in Section 4.5, a genetic optimization was found to be the most effective optimization algorithm that we tried, for calibrating the phase shifter values. A genetic optimization algorithm is one that uses the principles of random mutation and natural selection to optimize, in this case, the ADC input reading. Using simulated "generations" in the genetic optimization, we have shown an approximation for the optimal beamformer for 16, 32, 48 and 64 antenna elements as discussed in Chapter 5.

4.3 Digital Platform

To implement the beam steering of the electronically steerable antenna (ESA) we considered several types of processors. After we decided which type of processor we wanted, we looked at different commercial boards to implement the full beamsteering algorithm.

4.3.1 Processors Considered

Artix 7 [15]: This FPGA is a 7 series Xilinx product that Dr. Warnick's research group previously used to implement the Overhorizon beam-steering algorithm. This option would have used a soft-core processor design called a "MicroBlaze" to create the processor inside the FPGA fabric.

Zynq [16]: This is a 7 series System-on-Chip (SoC) created by Xilinx. It is a FPGA with an ARM processor on top. It is the same chip that is currently used in EcEn 330/390 class on Digilent's Zybo Board. This processor package is not the newest SoC on the market, but the newer chips increase our cost by giving us more speed and extra processing power, which is something we did not need.

Microcontroller: This option was left broader because it was easy to see that it was not the optimal choice. I wanted to compare the performance of a SoC to a family of chips because of some of the obvious problems discussed below. If I had to choose a board, I might have gone with the Raspberry Pi 3 as my option to compare.

Criteria

Development Platform: This decision metric was used to access how hard it would be to develop the beamforming algorithm considering the previous experience of my group. Xilinx based FPGAs use Vivado to program the FPGA which is a software package that I already had experience with. Intel-owned Altera is another FPGA manufacturer and their development platform is quite different from Vivado, though more user-friendly. Each microcontroller has a slightly different development platform, but they are similar to Arduinos software package.

Code Portability: This decision metric is an extension of the previous category but asks how much of the code could be ported from a previous project. The Navair project is similar to the Overhorizon project in many ways and the goal was to be able to port as much of the non-propitiatory code as possible. The goal here was to avoid having to re-invent the wheel.

Cost: The Navair project was relatively limited in funding and so I needed to be prudent.

Speed: This decision metric considered the maximum clock speed of the chosen processor.

Parallel Processing Power: Finally, this decision metric considered how many things can be done at once. The microcontrollers that were considered were all single core processors, so they were weak in this area. FPGAs excel in this area because with them I can create a circuit that calculates everything at the same time.

Processor Decision

The decision matrix was left out of this document, but the decision ended up with a close choice between the previous platform using the Artix7 and the new platform using the Zynq. I decided to move up to a slightly more powerful device and went with the Zynq. I already have access to the Artix7 so moving forward with the Zynq gave us exposure to both options.

4.3.2 Commercial Boards Considered

Arty A7 Board by Digilent [17]: This is the FPGA-based board that Dr. Warnicks research group used for the OverHorizon project and thus my team had a lot of experience with this board.

Microzed^{TM} [18]: This is a Zynq-based board is previously used in a collaborative C-UAS Drone Radar research project between Dr. Warnick, Dr. Beard, Dr. Wirthlin and Dr. Wilde. Kaleo Roberts described his use of this board in his thesis [19].

PicoZed^{TM} [20]: This option is very similar to the MicroZed without all of the peripherals. It has more IO and is smaller than the MicroZed. It would require a carrier card for programming and input/output.

Zybo Zynq-7000 Board [21]: This is a board that is currently being used in the Junior-Core to develop the EcEn 390 Laser Tag project. Having spent hours using this hardware in both EcEn 330 and 390, I wanted to see where it stacked up against the other boards.

Criteria

Previous Experience: The goal was to choose a platform that would allow me to get something working as soon as possible. This decision metric reflected mine and other research students' experience on the platform.

I/O: Input/Output is important because the Navair project goal was to drive multiple antenna tiles which could need as many as 100 I/O (the number was variable depending on design decisions). 100 I/O is actually kind of rare on commercial boards, so it was not a strict requirement as a decision metric, but it was still an important goal to shoot for.

Cost: We had a reasonable budget but like all engineering projects we need to be prudent.

Convenience: Finally, this decision metric tested how easy it would be to use the board. Some of the Boards I considered required a carrier card just to program the system. I thought this would be a waste of money and an inconvenience.

Board Decision

For various reasons, each of the other boards we considered dropped out and we were left with the MicroZed. This was a great option because Kaleo Roberts [19] and David Buck had previous experience to help us get started.

4.4 Programmable Logic: FPGA

Having chosen to work with the Zynq SoC, the remainder of this chapter will divide the software development into two main categories: programmable logic (PL) and the processing system (PS). These terms refer to the different parts of the Zynq using the terminology that Xilinx themselves uses. PL refers the FPGA fabric and PS refers to the ARM processor.

The firmware developed for the Navair project was similar to the Overhorizon project in many ways. Figure 4.2 shows the block diagram that was used in Vivado 2016.2 to program the PL of the Zynq. The following will describe the function of each of the blocks in Figure 4.2.

4.4.1 ZYNQ7 Processing System and Processor System Reset

The Zynq7 PS and reset blocks are the first two blocks of any Zynq-based design. As referenced in PG082 from Xilinx [22]

> The Xilinx LogiCORE IP Processing System 7 core is the software interface around the Zynq-7000 platform Processing System. . . . The Processing System 7 core acts as a logic connection between the PS and the PL while assisting you to integrate custom and embedded IP cores with the processing system using the Vivado Design Suite.

The Zynq7 Processing System allowed us to run software baremetal (see Section 4.5 for more details.) or without any kind of operating system. This block can do many of the AXI-based things that this design (ex. UART, SPI, and I2C) needed but after having trouble getting the UART working, I focused on AXI-based solutions for external communication. The UART capability of this block is how the user communicates with the Navair Software platform. The user connects via UART to the MicroZed and sends ascii characters back and forth through a commandline interface. The chosen UART settings for this communication were: Baud Rate = 115200 bps, Data = 8 bits, Stop = 1 bit, Parity = 1 bit. Figure 4.5 shows this in better detail.

The MicroZed has a local oscillator running at 33.33 MHz and within this block we set the necessary PLL to have 100 MHz be the reference clock for everything except the two different SPI blocks. Within this block we defined the SD Card pins and allowed for its use within the PS. The reset block grouped with this PS block is as simple as it sounds; it allows the design to control the resets throughout the design. The default settings were used to set up the reset block.

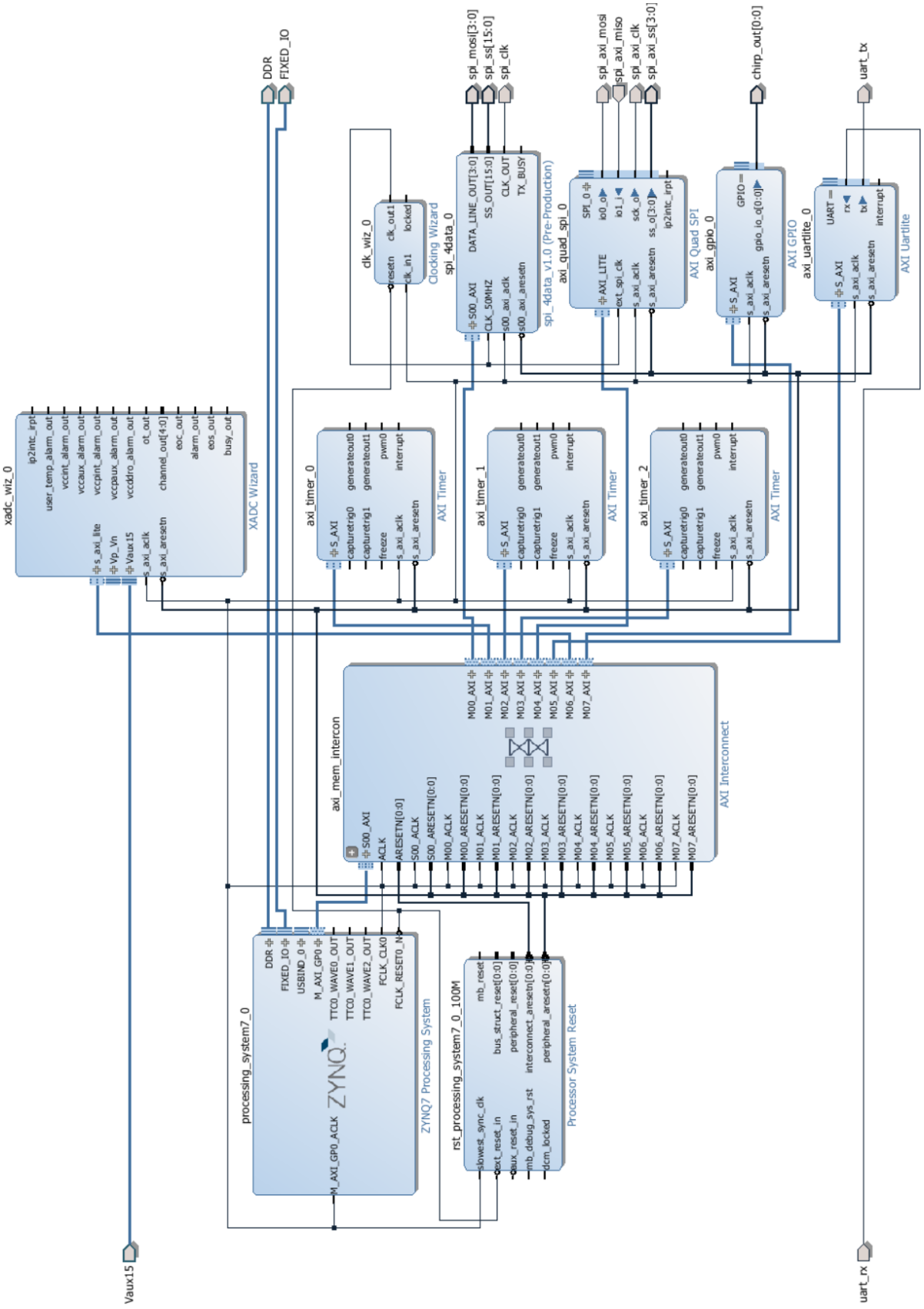

Figure 4.2: Trimmed Vivado block diagram showing only necessary block connections and I/O.

Table 4.1: AXI Memory Addresses, 32 address bits, start register: 0x40000000

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
axi_bram_ctrl_0	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF
axi_timer_0	S_AXI	Reg	0x4280_0000	64K	0x4280_FFFF
axi_timer_1	S_AXI	Reg	0x4281_0000	64K	0x4281_FFFF
axi_timer_2	S_AXI	Reg	0x4282_0000	64K	0x4282_FFFF
axi_intc_0	s_axi	Reg	0x4180_0000	64K	0x4180_FFFF
xadc_wiz_0	s_axi_lite	Reg	0x43C0_0000	64K	0x43C0_FFFF
axi_quad_spi_0	AXI_LITE	Reg	0x41E0_0000	64K	0x41E0_FFFF
axi_uartlite_0	S_AXI	Reg	0x42C0_0000	64K	0x42C0_FFFF
axi_gpio_0	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
spi_4data_0	S00_AXI	S00_AXI_reg	0x43C1_0000	64K	0x43C1_FFFF

4.4.2 AXI Interconnect

The AXI Interconnect block is the backbone (or rather the spinal cord) of this firmware design. This standard Xilinx-built IP core implements the Advanced Microcontroller Bus Architecture (AMBA®) standard version 4 for Master/Slave communication. PG059 contains detailed information about how to use this block [23]. This industry-standard block is used to communicate with each of the AXI-based blocks in the design. The memory addresses defined in Table 4.1 are the same memory addresses used in the baremetal software design. The address space is 32 bits with the start register starting at 0x40000000 after the dedicated addresses for the RAM. The Zynq PS block is the Master to this AXI bus, and all of the following AXI-based blocks are slaves to this AXI bus. This is what makes it possible to communicate with these blocks from the baremetal software.

4.4.3 AXI Timer

This design duplicates the AXI Timer design that exists in the current version of the EcEn 390 Laser Tag project. The Introduction to embedded programming course (EcEn 330) introduced us to using multiple timers together from a software perspective. This design uses three of these AXI Timers which are fully explained in PG079 [24]. While in EcEn 330, I developed code to work with these AXI Timers and was able reuse that code by building the firmware in this way.

4.4.4 AXI Uartlite

The AXI Uartlite block is used to send UART commands to the servo controller. PG142 gives specific details of how to use this block [25]. While by default UART is designed for two-way communication, this path is only used to transmit to the servo controller and the servo controller does not transmit back. For this reason, the receive pins are never actually connected on a hardware level. The servo controller is an Arduino board that accepts the azimuth and zenith angles sent as a string of ASCII characters. The chosen UART settings for this communication were: Baud Rate = 9600 bps, Data = 8 bits, Stop = 1 bit and no Parity bit.

4.4.5 XADC Wizard

The XADC Wizard 3.3 is used to instantiate usage of the on-board ADC module that is built into the Zynq Soc. Xilinx 7-series FPGAs have branded this ADC module as the XADC referring to their propitiatory hardware design, and the associated IP. PG091 gives specific details of how to use this block [26]. This block is used as an AXI slave and returns the signed 12-bit ADC value relative to +/- 1 volt. This ADC can be sampled up to 250 MHz but the Navair project only samples the ADC value when reading the relative power from the power detector which needed about every millisecond when calibrating.

4.4.6 AXI Quad SPI

This is the built-in SPI engine that was used to control the Radar Transmitter board. This functionality was needed to generate radar pulses without a signal generator. The project sponsor determined that this functionality was unnecessary. PG153 gives specific details of how to use this block [27].

4.4.7 Custom SPI engine: spi_4data

This custom IP core was developed as a SPI engine to drive the phase shifter chips (maps-010146) for the Navair project. This VHDL-based component is another AXI slave designed to specifically follow the given timing specifications in the MAPS-010146 datasheet [1]. Figure 4.3

and Table 4.2 show the given timing specifications from the v3 version of the datasheet, which was current at the time of writing. Figure 4.4 shows the settings that were developed for use of this custom IP core within Vivado 2016.2. The input boxes at the bottom of Figure 4.4 give the user access to generics, or parameters, in the HDL to customize the internal clock division (”Clk Div”), the number of Slaves (”Slave Count”) and the output bit resolution (”Output Data Bits”).

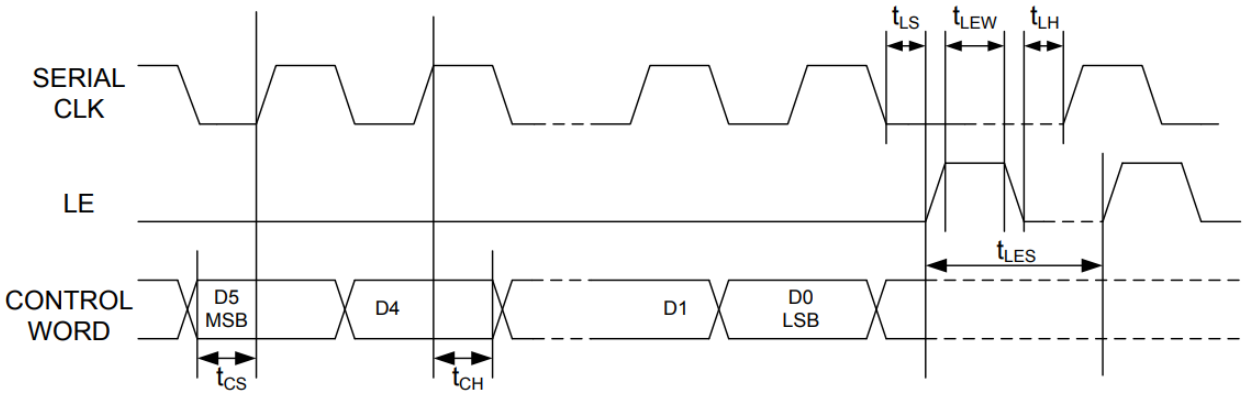

Figure 4.3: Phase Shifter Serial Input Interface Timing Diagram. [1]

Table 4.2: Phase Shifter Serial Interface Timing Characteristics for Figure 4.3 [1].

Symbol	Parameter	Typical Performance	Units
t_{SCK}	Min. Serial Clock Period	100	ns
t_{CS}	Min. Control Set-up Time	20	ns
t_{CH}	Min. Control Hold Time	20	ns
t_{LS}	Min. LE Set-up Time	10	ns
t_{LEW}	Min. LE Pulse Width	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	ns
t_{LES}	Min. LE Pulse Spacing	630	ns

4.4.8 Unused: AXI BRAM Controller and AXI Interrupt Controller

The AXI BRAM and AXI Interrupt Controller are legacy parts of the design that were unused in the Navair project. The AXI BRAM Controller allows access to the limited fast memory

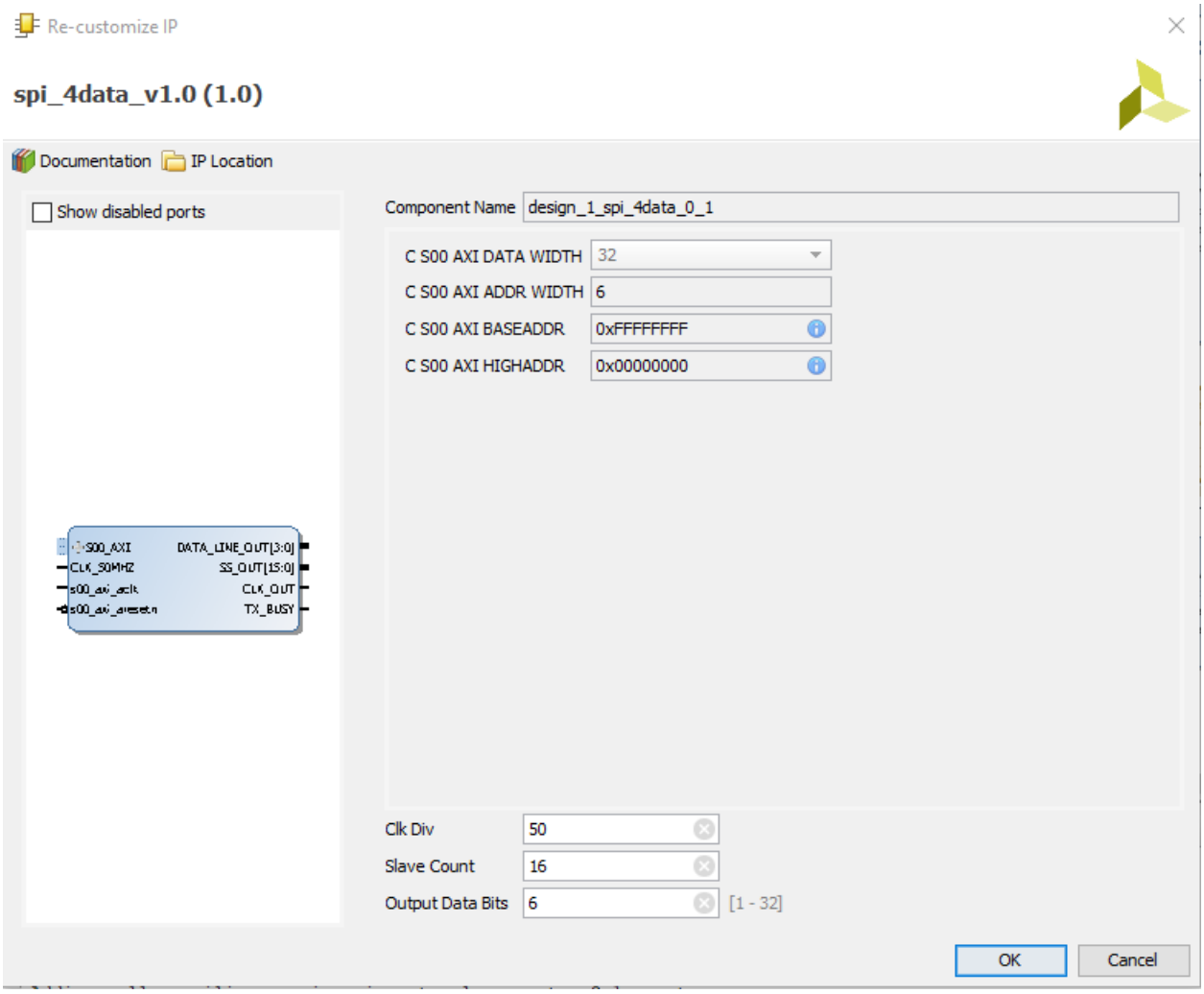

Figure 4.4: spi_4data_v1.0 settings GUI showing options to change the clock, the number of slaves and the number of output bits.

available inside of the PL itself. In the past this was used to initialize the detection algorithm. The AXI Interrupt Controller was added to make the design interrupt driven. In the past this was used for a better implementation of tracking. The feature of having an interrupt driven design was determined to be unnecessary. These blocks are not pictured in Figure 4.2.

4.5 Processing System: Baremetal Software

The bare metal software includes several C classes interacting together. The *main.c* calls the *ui.c* (user interface) class which contains a series of console-based menus that call the various operational functions. The user interface used the serial UART settings shown in Figure 4.5. We

use the Putty client to manage our serial communications in this project, but many other packages are available. The user interface command prints menu items to the Putty terminal with associated keys; the user responds by typing the associated keys.

We programmed the MicroZed to directly read and write files to the SD card. This allowed us to load configuration files, as well as store test data. The SD card can be manually transferred to a host PC for further data manipulation. We hope to improve this interface with the network transfer protocols available in a future operating system platform.

Class descriptions

In this section we provide a brief description about the contents of each class.

- **main**

  Initializes the various peripherals and classes.

  Calls the ui class.

  Cleans up allocated memory on exit.

- **ADC**

  Interacts with the MicroZed's XADC module in the PL to sample the power detector output.

- **calibrationRoutines**

  Various optimization methods used to search for optimum phase states with environmental uncertainties. The most successful of these was the genetic optimization algorithm.

- **fast_math**

  Various numerical methods used to speed up computation (such as sin and cos in lookup tables).

- **files**

  Custom FAT32 file system that is used to write and read from the SD card.

- **geom**

  A collection of functions for generating equidistant spherical points across the field of view.

- **phaseshifter**

  Programs the phase-shifters in each tile using the spi4data class.

- **servo**

  Programs the servo positioner to physically move the tiles in the test chamber.

- **skyPointsLUT**

  This class contains the central data structure containing the power levels and optimum phase-states at each point in the sky.

  The memory contained in this database is allocated dynamically on boot-up.

  This database can be dumped and loaded from the SD card.

- **spi_4data_custom**

  Contains various function for interacting with other peripherals in the system.

- **transmitter**

  Control functions for the stand-alone transmitter source.

- **ui**

  Various menus that link to operational functions.

  This class contains most of the routines that call the other functions including demonstration code.

The calibrationRoutines class works with the associated data structures to run the needed optimization to perform analog adaptive beamforming. All the needed processing is accomplished on the embedded platform (MicroZed) without the use of an operating system.

4.6 Summary

The software platform presented in this chapter was used to drive the hardware described in Chapter 3 to demonstrate analog adaptive beamforming with multiple phased array antenna systems using a "zero-knowledge" approach. After considering multiple options, we chose the Zynq-based Microzed as the digital controller for this project because of the many user configurable I/O pins. Choosing a Xilinx SoC gave us both the parallel nature of an fpga combined

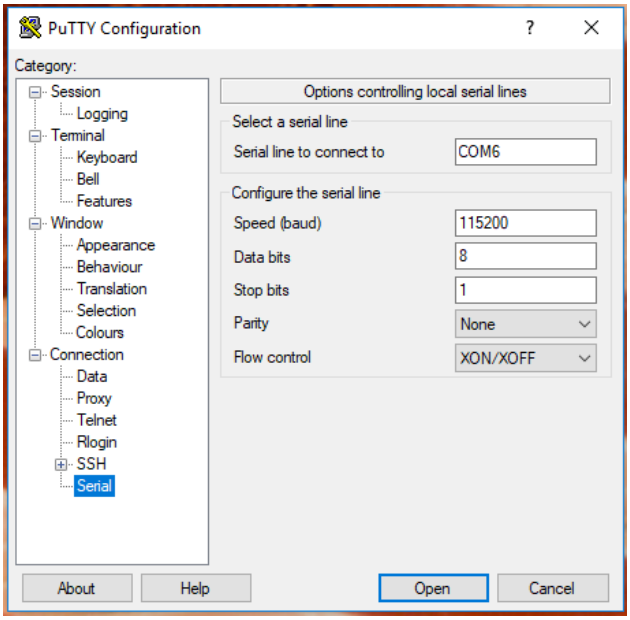

Figure 4.5: Settings for communicating with the MicroZed board over serial UART using the Putty client.

with an ARM core processor for higher level processing. Both the fpga fabric and processor were efficiently used to allow this software platform to be used in the future phase of this project.

CHAPTER 5. EXPERIMENTAL RESULTS

The previous chapters have described the hardware design and the software development for an aggregated system consisting of multiple phased array antenna systems. One of the most important aspects of this system's development was the capability it demonstrated to effectively beamform. Even in our modest antenna chamber, antenna beam pattern measurements demonstrated analog adaptive beamforming. The results in this chapter show a close agreement between simulated and measured results.

5.1 Antenna Chamber

The tests for the Navair project were conducted in the Microwave lab on the 5th floor of the Clyde Building on BYU campus. In the Microwave lab, the Smart Antenna Systems (SAS) group built a simple anechoic chamber for antenna testing. The chamber is roughly 10 x 6 x 6 feet and uses RF absorber foam on the inside. The chamber and associated servo arm are not calibrated to give precise antenna measurements, but the results of this chapter show that this chamber, though simple, is good enough for student projects.

5.2 Experiment Setup

We initially performed our tests with the arrangement seen in Figure 5.1. This figure shows a single antenna tile connected to a servo arm. The servo arm was a daisy chain of Dynamixel MX-64 servos controlled by a generic Arduino (originally an Arduino UNO). The MicroZed sends a UART command of elevation and zenith to the Arduino which parses the command and then sends pulse width modulated (PWM) signals to each of the servos.

The RF signal path starts at the back of the antenna tile before the T-divider board. In the case of more than one tile, an RF splitter was used to bring the input signal to each tile. This input signal was generated using one of two methods: a high quality signal generator or the radar chirp

generator board shown in Figure 5.1. The latter of these was included in the design with mobility of the hardware in mind but our sponsor, Navair, decided that this functionality was unnecessary for the project. Thus, we set a signal generator to 10.25 GHz with enough power to compensate for cable loss such that 18 dBm of RF power arrived at the T-divider input.

After being split by the T-divider, each output was connected to a blade which had the phase shifter and an amplifier chain that brought the transmit power back up to 18 dBm per channel, or 1 Watt radiated per antenna tile. This RF signal was then received by a dual polarized horn antenna located at the back of the anechoic chamber. The aligned polarization SMA output is connected with a long low-loss cable to a mixer as the RF input. The 10 GHz signal was mixed down to a 2 GHz intermediate frequency (IF) using a second signal generator set to 8 GHz with adequate power to drive the mixer (about +7 dBm compensated for cable). This 2 GHz IF signal is directly connected (with or without filtering) to the linear power detector board. The power detector generated a discrete voltage that was proportional to the input RF power. To protect the MicroZed we used a resistor divider network to lower the output voltage to be within the +/- 1 voltage range for the MicroZed's onboard ADC.

Our setup improved throughout the Navair project and most of the individual boards were grouped together in a more professional way. We wired up the subsystems in the final demonstration according to Figure 5.2. The wiring documented in this figure shows the final product with four antenna tiles all being controlled by the MicroZed.

5.3 Beam Pattern Measurements

Antenna beam patterns were measured using the anechoic chamber shown in Figure 5.1. This uncalibrated chamber gave us a baseline to show impressive beamforming results.

5.3.1 Simulation

The simulation used in Figures 5.5, 5.9, and 5.10 was developed in Matlab using techniques taught in EcEn 665 taught by Dr Warnick. Both the classical array factor method and the overlap integral were compared and used in this simulation. Mutual coupling between arbitrarily located array elements was not found to be a significant issue because the mutual coupling decreased as

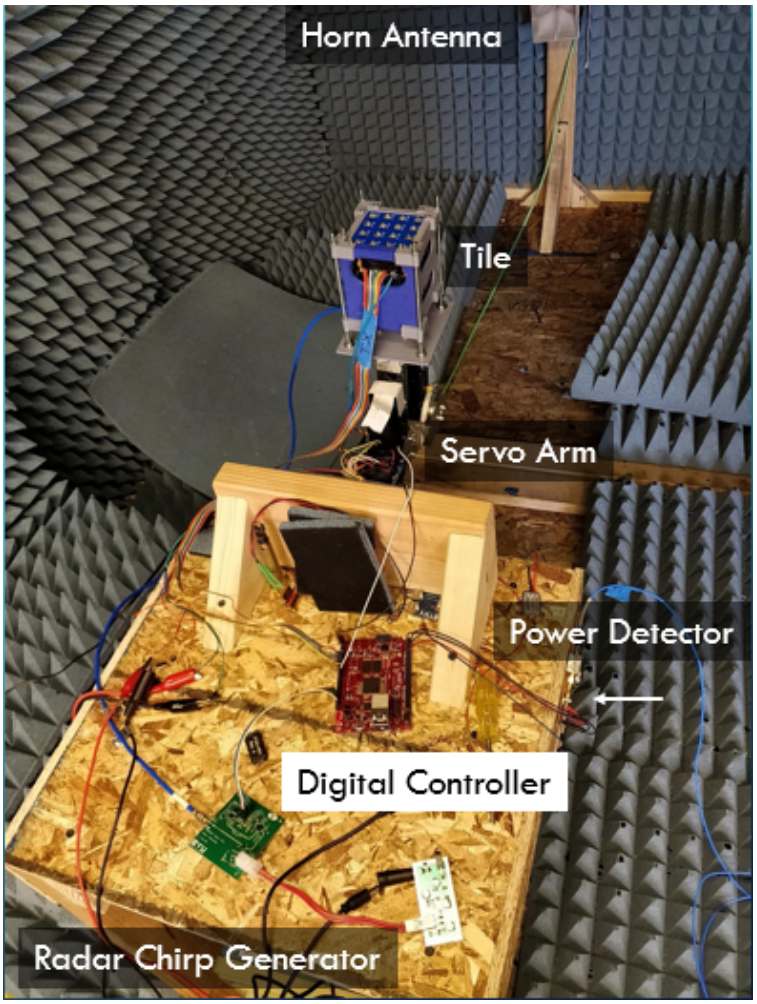

Figure 5.1: Single antenna tile test setup inside the anechoic chamber.

the antenna tiles were spaced farther apart. Conjugate Field Match (CFM) weights were used for the overlap integral approach.

Simulation results were used to determine spacing between the antenna tiles in the creation of the 3D-printed enclosure. We found that increasing the spacing between antenna tiles created a "fingered" mainlobe with many extra nulls. Figure 5.3 shows the effect of this fingered pattern and how it slices up the desired mainlobe. The optimal spacing is simply to skip one element in the ULA, effectively making the four tiles perform like a 9x9 ULA with the middle column and row removed. This optimal spacing was used in the creation of the 3D printed box and was shown to be successful.

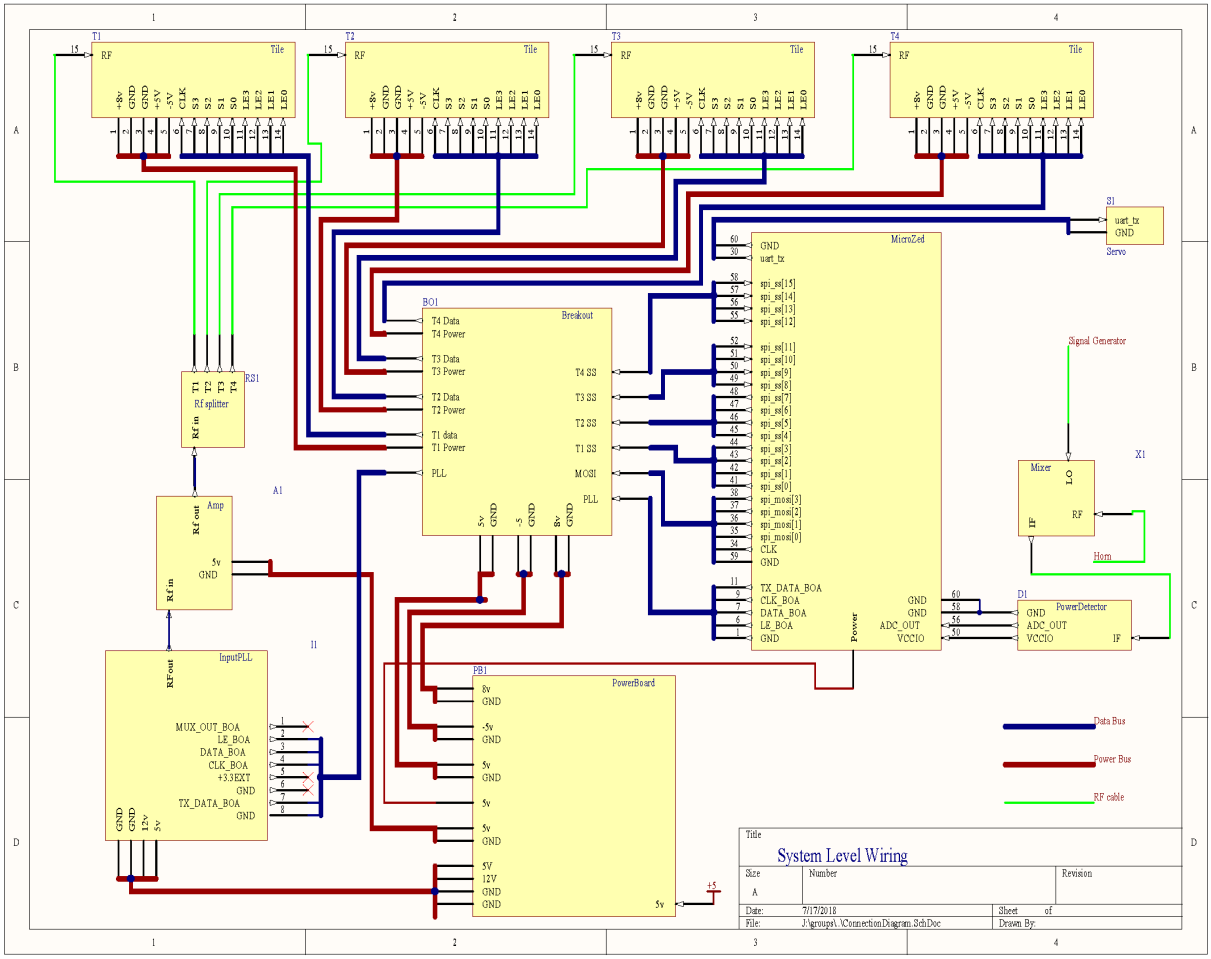

Figure 5.2: Connection diagram of our system-level testing in the anechoic chamber.

5.3.2 Two Antenna Tiles Steered to BoreSight

After integrating two tiles in the chamber, our first test demonstrated successful integration by measuring the antenna pattern of the combined array. This first test followed this procedure:

- Move the servo to face boresight to the receiving antenna
- Perform a genetic algorithm calibration to search for a max-power phase-state
- Save the search results, program the phase shifters to this phase-state
- Move the servo around the hemisphere, sampling the power detector at each location
- Save and export the power detector's ADC codes to Matlab via the removable SD card

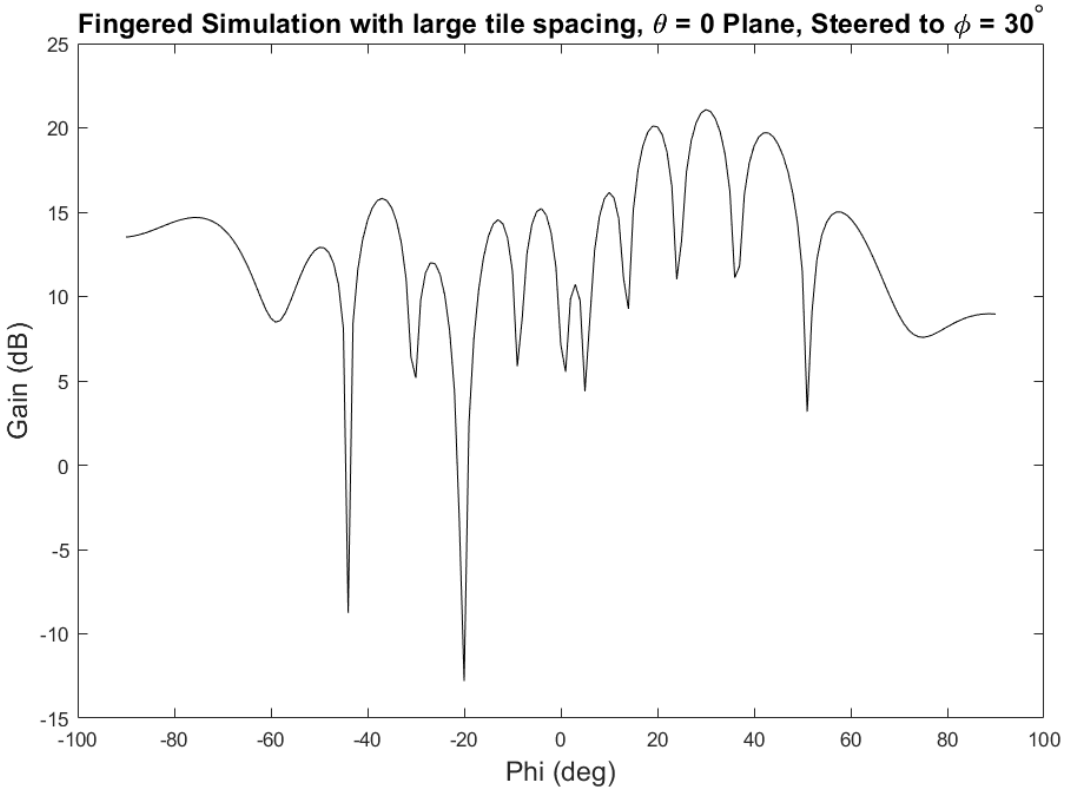

Figure 5.3: Fingered Simulation with tiles separated by 5 element spacings (5*0.55λ), This is a zenith slice where $\theta = 0$ and the beam is steered to $\phi = 30°$. This shows a very distorted mainlobe that is barely above the sidelobes.

After loading the ADC codes into Matlab, we mapped the ADC codes to power levels in the detector. This mapping was required to interpret the measured power from the detector. The power detector provided a voltage proportional to input power. An ADC sampled a scaled version after passing the power detector voltage through a resistor divider network. Because several systems were interacting together, the most direct way to derive the mapping came from experimental measurements with controlled input powers into the detector. By using a signal generator to insert a known signal into the power detector and by recording the corresponding ADC codes, we produced the mapping as shown in Figure 5.4.

After applying the mapping between ADC codes and power levels, we had the received power at each direction in the hemisphere. These data were not fully useful for quantifying the array's antenna performance because received power is dependent on the receiver's distance and signal gain. To isolate the array's antenna performance, we performed a further step to normalize

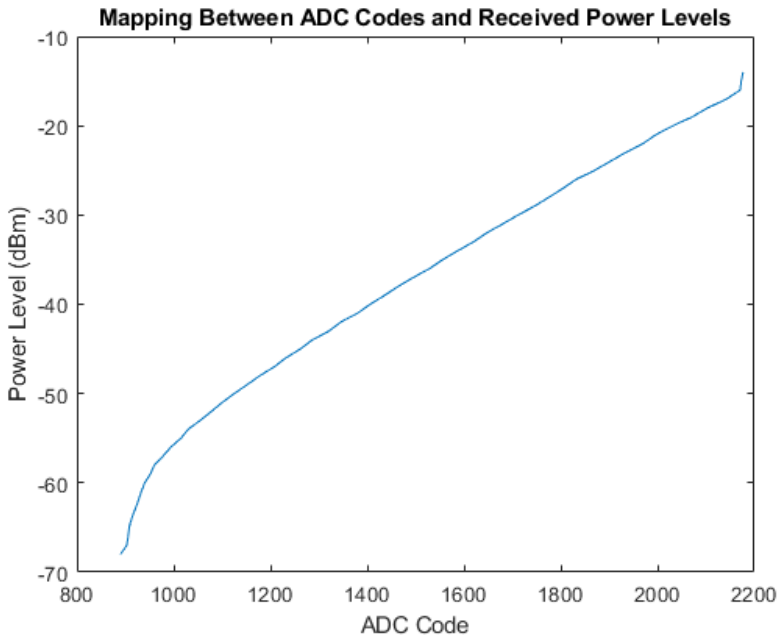

Figure 5.4: Relationship between ADC codes and power level into the power detector taken from controlled measurements with a signal generator.

the data in terms of antenna gain. Antenna gain is a measure of power intensity measured by an antenna in reference to the power intensity of an ideal antenna that radiates equally in all directions (isotropic radiator). Antenna gain changes over direction and is defined by

$$G(\phi,\theta) = \frac{P_{ant}(\phi,\theta)}{P_{iso}}. \tag{5.1}$$

Our measured data provided an estimate of P_{ant}, but we did not have a power measurement for P_{iso}, so we had to estimate it from the measured data. P_{iso} is defined as:

$$P_{iso} = \frac{TotalRadiatedPower}{SurfaceArea}$$

$$P_{iso} = \frac{\int^{\Theta}\int^{\Phi} P_{ant}(\phi,\theta)d\phi d\theta}{\int^{\Theta}\int^{\Phi} d\phi d\theta}. \tag{5.2}$$

With discrete $P_{ant}[\phi,\theta]$ we estimate P_{iso} with a sample mean

$$\bar{P_{iso}} = mean(P_{ant}[\phi,\theta]). \tag{5.3}$$

Using Equation 5.3 with Equation 5.1 we estimate the pattern gain

$$\bar{G}[\phi,\theta] = \frac{P_{ant}[\phi,\theta]}{mean(P_{ant}[\phi,\theta])}. \tag{5.4}$$

In our measurement, we were only able to measure power over points on a hemisphere, so our estimate of antenna gain assumed that negligible power radiates in non-hemisphere directions. We justified this assumption with simulated gain values on the order of -100 dB outside of the hemisphere.

After applying our antenna gain estimate to our measured data, we produced the plot shown in Figure 5.5. This plot shows measured gain vs simulated gain on a slice across the main axis. This slice contains the main features of the boresight antenna pattern. We found the peak side lobe level was lower than expected. This suggests that the genetic algorithm may have found a phase-state with reduced side lobes compared to simulated conjugate match.

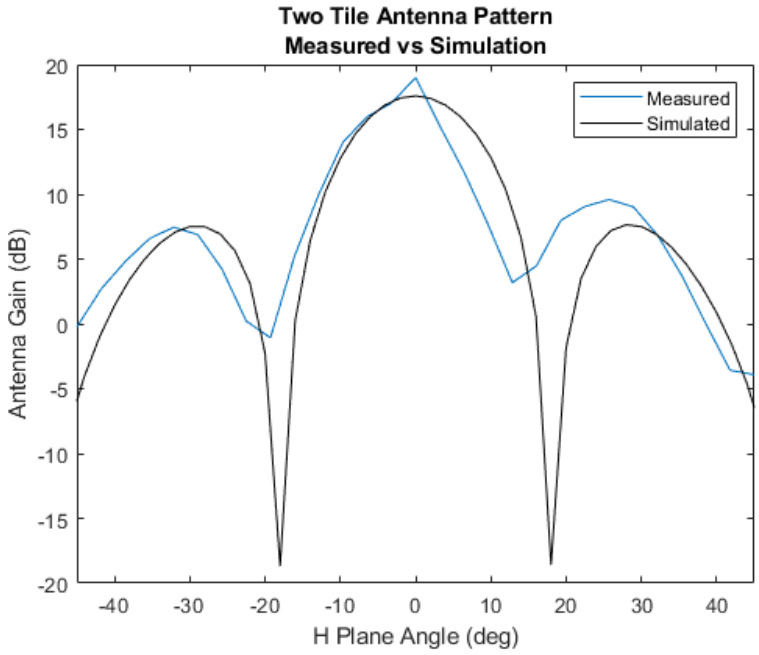

Figure 5.5: A comparison of the measured antenna gain to simulated antenna gain which demonstrates the validity peak gain measurement, correct location of side lobes, and also suggests that the genetic algorithm search may have found a phase-state with reduced side lobes compared to the standard conjugate match beam-former weights.

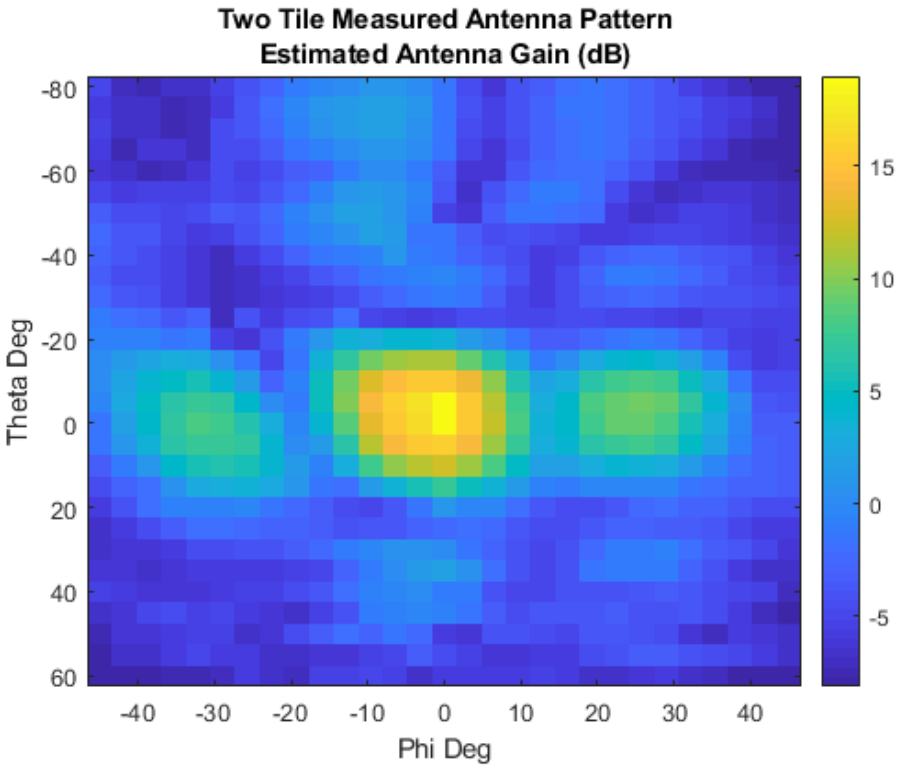

Figure 5.6: Relationship between ADC codes and power level into the power detector taken from controlled measurements with a signal generator.

5.3.3 Four Antenna Tiles

Building off the analysis developed in the previous section, three tiles were provisionally tested before finally combining four antenna tiles as shown in Figure 5.7. This system demonstrated effective beamsteering to the project sponsor, Navair, on October 17th, 2018. Figure 5.8 shows the updated antenna test setup in the same antenna chamber as Figure 5.1.

Figures 5.9 and 5.10 show a zenith cut at $\theta = 0^\circ$ of the antenna beam pattern with the beam steered to boresight (Figure 5.9) and with the beam steered to $\phi = 30^\circ$(Figure 5.10). These beam pattern measurements are both compared to their respective simulation as discussed in Section 5.3.1. Both measurements show a strong correlation with the simulated beam pattern. Specifically, the Null-to-Null beam width is measured to be within one degree of simulation. Both Figures 5.9 and 5.10 have different sidelode heights than expected from simulation.

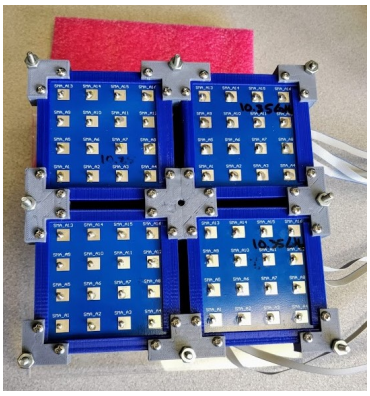

Figure 5.7: Four Functional Antenna Tiles combined using a 3D printed case.

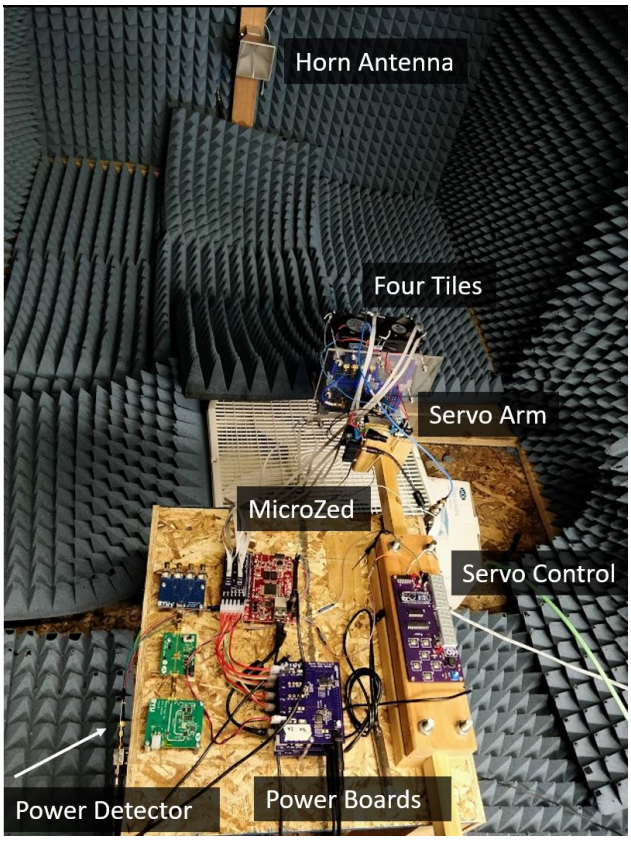

Figure 5.8: Updated Test setup with four tiles showing the system as shown in Figure 5.2.

The differences in sidelode heights could be one of multiple differences including:

- Antenna chamber calibration: The simple setup used for these measurements was uncalibrated and easily could have introduced bias through the servo motion/calibration and near-field effects

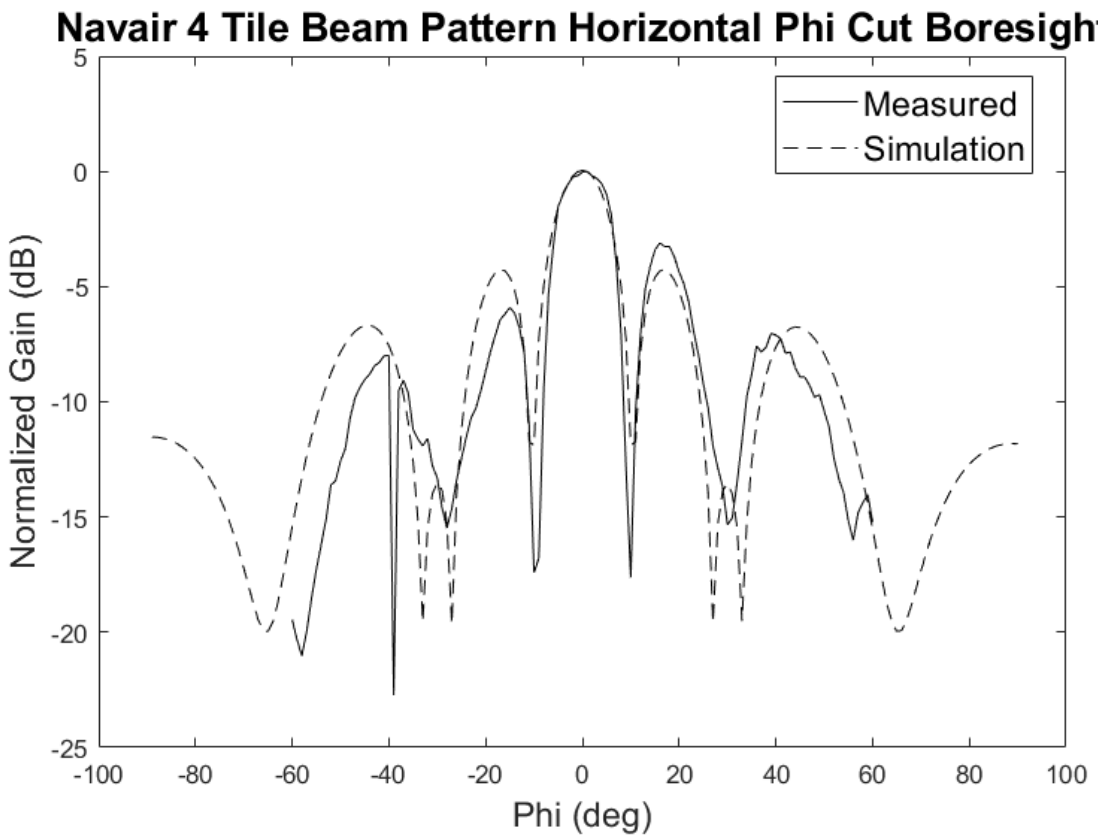

Figure 5.9: A normalized comparison of the measured antenna directivity to simulated antenna directivity which demonstrates the correct beamwidth and correct location of side lobes.

- Optimization result: The genetic optimization only considered the mainlobe and tried to maximize the directivity. The optimization could have arrived at phasestate that raised one sidelobe above another through random mutation.
- Experimental error: relative power levels fluctuated within a 3dB tolerance. Refer to the not-flat sensitivity map in Figure 5.11.

These findings were not explored deeper because sidelobe structure and height were not listed as a priority by the project sponsor. Navair was much more interested in demonstrating maximum directivity with arbitrary antenna element positions.

The null in Figure 5.9 near -40 degrees was probably due to inadequate cooling during that specific ADC sample. With four antenna tiles, we started seeing signal dropouts as the whole system heated up (after about 20 minutes of operation). Adding fans (pictured in Figure 5.8) lowered the frequency of these dropout events but did not entirely remove the problem. After

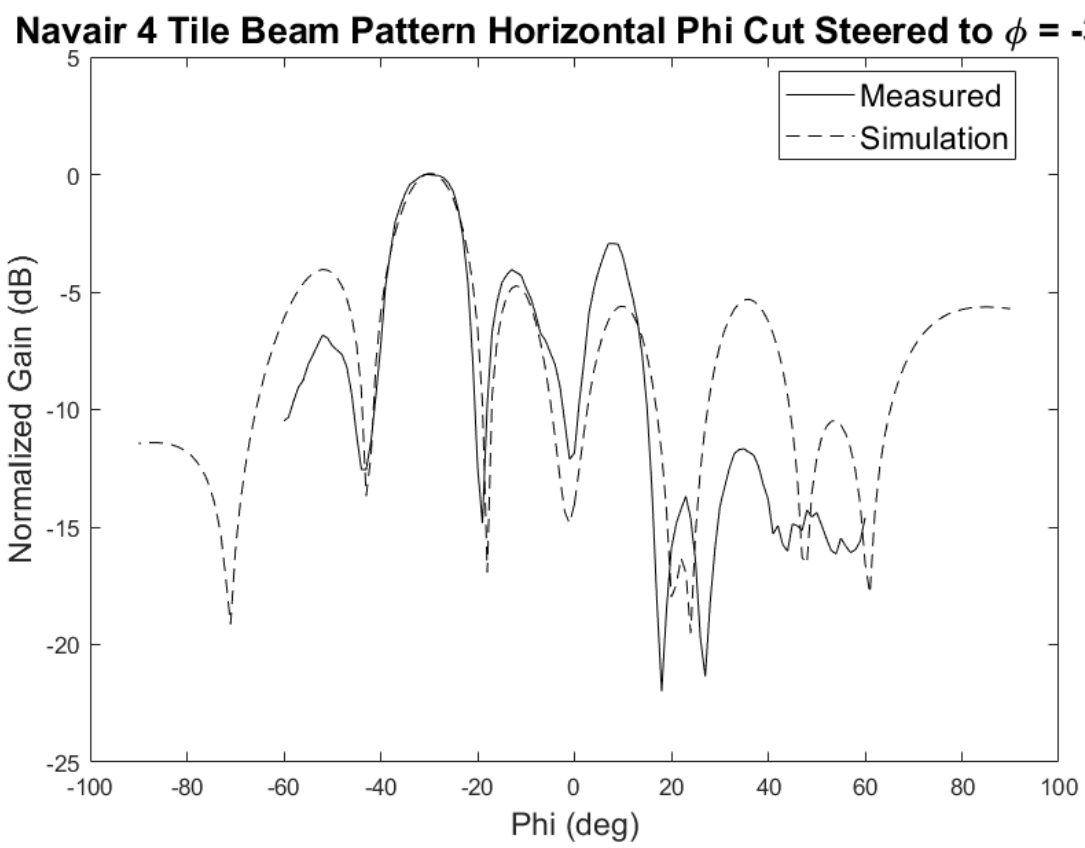

Figure 5.10: A normalized comparison of the measured antenna directivity to simulated antenna directivity both steered to 30 degree which demonstrates the ability to steer the beam, the correct beamwidth and correct location of side lobes.

checking and rechecking the hardware, our understanding was that the RF amplifier chains were simply overheating which greatly reduced their gain. Signal was indeed still present during these dropout events but dropped below the sensitivity of our power detector board.

Figure 5.11 shows a simple relative measured versus simulated sensitivity map of the Navair four-tile transmitter between +/- 30 degrees on five degree increments. This system has no characterization of the noise, so this sensitivity is simply relative and not the true sensitivity. The y-axis is the normalized gain in dB. This plot should be much flatter than shown with shoulders as the system moves farther from boresight. Each of these 13 points was an individual calibration so the previous list of possible explanations still applies. However, an agreement within 4 dB is a valid result for the error we were working with.

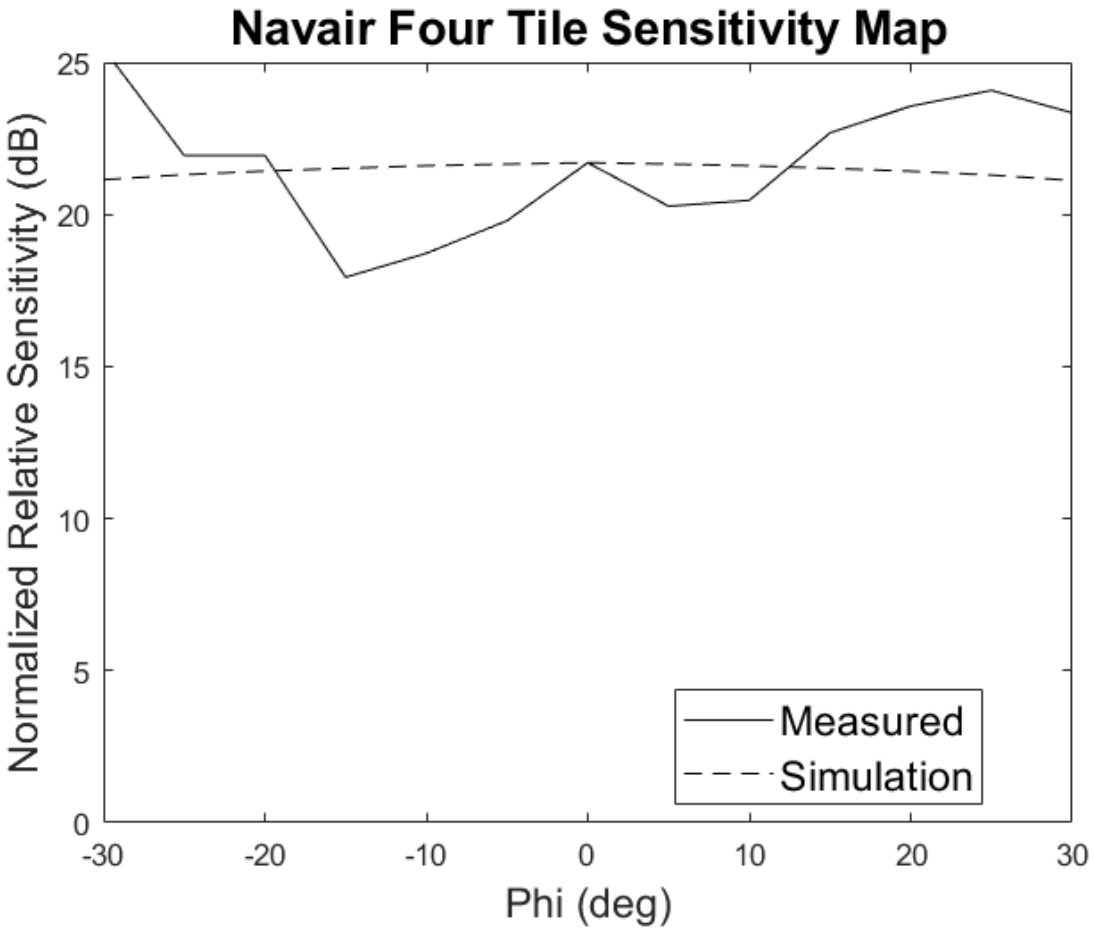

Figure 5.11: The measured versus simulated sensitivity map of 13 steered locations on 5 degree increments. This plot shows that the gain is between 18 dB and 24 dB and while not flat as expected, the variation is understandable due to experimental error.

CHAPTER 6. CONCLUSION

6.1 Conclusion

This work has demonstrated the feasibility of building a modular phased array antenna system for Navair. Using relatively limited resources, we aggregated four antenna tiles, each consisting of a 4x4 antenna array, to seamlessly work together in a combined phased array antenna system. This work has developed and discussed the successful implementation of an adaptive analog beamformer calibration algorithm that allows for an arbitrary antenna configuration with variable number of antenna elements and locations. This system has been shown to approximate the maximum directivity beamformer. To demonstrate this approach, we built four working 4x4 phased array antenna tiles and tested them together in arbitrary configurations to show the viability of developing a physically reconfigurable system.

6.2 Future Work

Navair has provisionally funded a second phase of this project in the hopes of expanding the EIRP capability. The goal of the second phase of funding is to create more antenna tiles and to increase the 1 dB compression point, or simply the available power output, of each of the blades. The second goal is to integrate our embedded platform with their communication protocol for use at their test facility. The goal of this second phase of funding is to demonstrate working hardware on the Navair Electronic Warfare test range.

This second phase of the project will require considerable hardware work, but limited changes are needed for the digital system. The MicroZed has enough I/O to drive over eight fully functional antenna tiles from this project so a major change in digital platform is not advised. The following needs to be considered for scaling up the hardware:

- **Blade Redesign**: Multiple problems plagued the current blade design all the way through the design. One of the more painful mistakes that should be avoided is the use of MACOM's RF amplifier (MAAM-011101). This amplifier is very cheap and has a small footprint, but multiple problems were identified with this specific part and industry engineers advised us against using it a little too late in the game. Phase 2 of this project should redesign the blade to have a single amplifier with a higher 1 dB compression point.

- **Cooling the Transmit System**: Passive cooling was considered during the design process but not accurately modeled. The current system consumes close to 13 watts per antenna tile, but that will change a lot with a blade redesign. The single tile and two tiles tests were successful without external cooling. It was found that the four-tile system would overheat after about twenty minutes of use and fans were needed to cool the system down. Moving to higher power and more tiles means that cooling needs to be considered from the beginning of the project design.

- **Accurate Servo Movement**: The current four tile system weighs about 4 kg and has proved heavy enough to burn out expensive high torque servo motors. A larger system would not be possible to move with the servo arm configuration that was used in this project. A clever redesign would be necessary, possibly a rotating table.

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